

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, CORNHOLE, K19

PVT 04/24/2009

| REV | ZONE | ECN | DESCRIPTION OF CHANGE | CK APPD DATE | ENG APPD DATE |
|-----|------|-----|-----------------------|-----------------|------------------|
| ? | | ? | ? | ? | ? |

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| 4 | 4 | Power Block Diagram | N/A | N/A |
| 5 | 5 | BOM Configuration | DDR | 12/18/2008 |
| 6 | 6 | JTAG Scan Chain | DDR | 07/22/2008 |
| 7 | 7 | Functional / ICT Test | N/A | N/A |
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| 31 | 34 | Right Clutch Connector | MUXGFX | 12/08/2008 |
| 32 | 35 | SECUREDIGITAL CARD READER | VEMURI | 01/30/2009 |
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| 48 | 55 | Thermal Sensors | YUN_K19_MLB | 12/22/2008 |
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| 86 | 98 | LCD Backlight Support | YITE_M98_MLB | 07/02/2008 |
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ALIASES RESOLVED

Schematic / PCB #'s

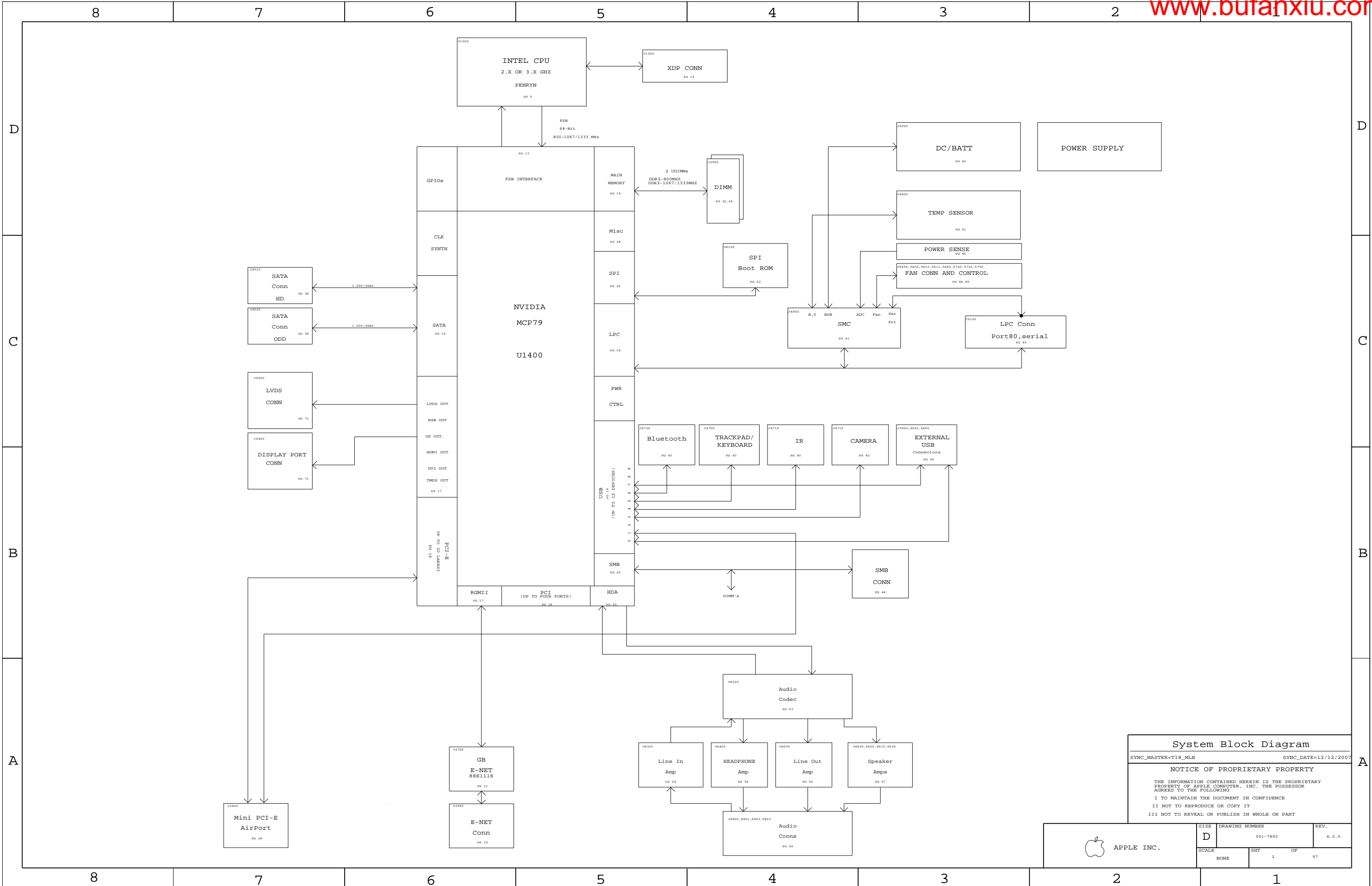
| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|--------------------|---------------|----------|------------|
| 051-7892 | 1 | SCHEM,CORNHOLE,K19 | SCH | CRITICAL | |
| 820-2523 | 1 | PCBF,CORNHOLE,K19 | PCB | CRITICAL | |

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TITLE
LAST_MODIFIED=Fri Apr 24 15:23:24 2009

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| DO NOT SCALE DRAWING | | DRAPTER | DESIGN CK | TITLE | |
| | | ENG APPD | MFG APPD | | |
| | | QA APPD | DESIGNER | | |
| | | RELEASE | SCALE | DRAWING NUMBER | |
| | | | NONE | 051-7892 | |
| | | MATERIAL/FINISH NOTED AS APPLICABLE | | SIZE | REV. A.0.0 |
| | | | | | SHT 1 OF 97 |



THIRD ANGLE PROJECTION



System Block Diagram

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

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BOM Variants

| BOM NUMBER | BOM NAME | BOM OPTIONS |
|------------|---|---|
| 630-9965 | PCBA, 2.66GHZ, 256SAM_VRAM, HB_AUDIO, K19 | K19_COMMON, DEVEL_BOM, EEE_6XN, CPU_2_66GHZ, FB_256_SAMSUNG |
| 630-9966 | PCBA, 2.66GHZ, 256HYN_VRAM, HB_AUDIO, K19 | K19_COMMON, DEVEL_BOM, EEE_6XP, CPU_2_66GHZ, FB_256_HYNIX |
| 630-9967 | PCBA, 2.80GHZ, 512SAM_VRAM, HB_AUDIO, K19 | K19_COMMON, DEVEL_BOM, EEE_6XQ, CPU_2_80GHZ, FB_512_SAMSUNG |
| 630-9968 | PCBA, 2.80GHZ, 512HYN_VRAM, HB_AUDIO, K19 | K19_COMMON, DEVEL_BOM, EEE_6XR, CPU_2_80GHZ, FB_512_HYNIX |
| 630-9969 | PCBA, 3.06GHZ, 512SAM_VRAM, HB_AUDIO, K19 | K19_COMMON, DEVEL_BOM, EEE_6XS, CPU_3_06GHZ, FB_512_SAMSUNG |
| 630-9970 | PCBA, 3.06GHZ, 512HYN_VRAM, HB_AUDIO, K19 | K19_COMMON, DEVEL_BOM, EEE_6XT, CPU_3_06GHZ, FB_512_HYNIX |
| 085-0736 | K19 MLB DEVELOPMENT | K19_DEVEL_PVT |

K19 BOM Groups

| BOM GROUP | BOM OPTIONS |
|---------------|---|
| K19_COMMON | ALTERNATE, COMMON, K19, K19_COMMON1, K19_COMMON2, K19_PROGPARTS |
| K19_COMMON1 | BOOT_MODE_USER, DPMUX_EN_S0, DP_CA_DET_EG_PLD, DP_ESD, EG_PWRSEQ_HW, EXTRACT_BUFF |
| K19_COMMON2 | GMUX_lvl8, GPUVID_1P00V, GPU_SS_INT, ISL6258A, MCP_B03, MCPSEQ_SMC, MIKEY, MUXGFX, SMC_DEBUG_YES, XDP |
| K19_DEVEL_ENG | BMON_ENG, DEBUG_ADC, GMUX_JTAG, LPCPLUS, VREFMRGN, XDP_CONN |
| K19_DEVEL_PVT | BMON_PROD, LPCPLUS, NO_VREFMRGN, XDP_CONN |
| K19_PROD | BMON_PROD, LPCPLUS_NOT, NO_VREFMRGN |
| K19_PROGPARTS | GMUX_PROG, BOOTROM_PROG, SMC_PROG, TPAD_PROG |

| BOM GROUP | BOM OPTIONS |
|----------------|-------------------------|
| FB_256_SAMSUNG | VRAM4, VRAM_256_SAMSUNG |
| FB_256_HYNIX | VRAM4, VRAM_256_HYNIX |
| FB_512_SAMSUNG | VRAM4, VRAM_512_SAMSUNG |
| FB_512_HYNIX | VRAM4, VRAM_512_HYNIX |

Bar Code Labels / EEE #'s

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|----------------------------------|---------------|----------|------------|
| 826-4393 | 1 | LBL, P/N LABEL, PCB, 28MM X 6 MM | [EEE:6XN] | CRITICAL | EEE_6XN |
| 826-4393 | 1 | LBL, P/N LABEL, PCB, 28MM X 6 MM | [EEE:6XP] | CRITICAL | EEE_6XP |
| 826-4393 | 1 | LBL, P/N LABEL, PCB, 28MM X 6 MM | [EEE:6XQ] | CRITICAL | EEE_6XQ |
| 826-4393 | 1 | LBL, P/N LABEL, PCB, 28MM X 6 MM | [EEE:6XR] | CRITICAL | EEE_6XR |
| 826-4393 | 1 | LBL, P/N LABEL, PCB, 28MM X 6 MM | [EEE:6XS] | CRITICAL | EEE_6XS |
| 826-4393 | 1 | LBL, P/N LABEL, PCB, 28MM X 6 MM | [EEE:6XT] | CRITICAL | EEE_6XT |

Module Parts

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|---|----------------------------|----------|------------------|
| 337S3761 | 1 | IC, FDC, SUGLA, FRQ, 2.66G, 256, K19, 3M, BGA | U1000 | CRITICAL | CPU_2_66GHZ |
| 337S3682 | 1 | IC, FDC, SUGEN, FRQ, 2.80G, 256, K19, 3M, BGA | U1000 | CRITICAL | CPU_2_80GHZ |
| 337S3744 | 1 | IC, FDC, SUGEN, GS, 3.06G, 256, K19, 3M, BGA | U1000 | CRITICAL | CPU_3_06GHZ |
| 338S0710 | 1 | IC, MCP79MXT-B3, 35X35MM, BGA1437 | U1400 | CRITICAL | MCP_B03 |
| 338S0694 | 1 | IC, RTL8251CA-VB-QR, OTDR TRANSCEIVER, 48P 1QFP | U3700 | CRITICAL | |
| 338S0654 | 1 | IC, FMS43-E, 1394B PHY/DMC1 L2BK/PCI-E, 12 | U4100 | CRITICAL | |
| 341S2384 | 1 | IR, ENCORE II, CVC63803-LQNC | U4800 | CRITICAL | |
| 338S0563 | 1 | IC, SMC, HSB/2117, 9MMX9MM, TLP | U4900 | CRITICAL | SMC_BLANK |
| 341S2462 | 1 | IC, SMC, DEVELOPMENT, K19 | U4900 | CRITICAL | SMC_PROG |
| 341S2503 | 1 | IC, PSOC +M/USB, 56PIN, MLP, K19 | U5701 | CRITICAL | TPAD_PROG |
| 335S0384 | 1 | IC, 32BIT 8-PIN SPI SERIAL FLASH, 901C8 | U6100 | CRITICAL | BOOTROM_BLANK |
| 341S2456 | 1 | IC, EFI ROM, DEVELOPMENT, K19 | U6100 | CRITICAL | BOOTROM_PROG |
| 338S0554 | 1 | IC, GPU, 55nm, NV G96-GS, BGA969, LF | U8000 | CRITICAL | |
| 333S0507 | 4 | IC, SDRAM, GDDR3, 16Mx32, 1000MHZ, 136 FBGA | U8400, U8450, U8500, U8550 | CRITICAL | VRAM_256_SAMSUNG |
| 333S0483 | 4 | IC, SDRAM, GDDR3, 16Mx32, 900MHZ, 136 FBGA | U8400, U8450, U8500, U8550 | CRITICAL | VRAM_256_HYNIX |
| 333S0511 | 4 | IC, SDRAM, GDDR3, 32Mx32, 800MHZ, 136 FBGA | U8400, U8450, U8500, U8550 | CRITICAL | VRAM_512_SAMSUNG |
| 333S0506 | 4 | IC, SDRAM, GDDR3, 32Mx32, 900MHZ, 136 FBGA | U8400, U8450, U8500, U8550 | CRITICAL | VRAM_512_HYNIX |

Development BOM

| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|---------------------|---------------|----------|------------|
| 085-0736 | 1 | K19 MLB DEVELOPMENT | DEVEL | CRITICAL | DEVEL_BOM |

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS: |
|-------------|---------------------------|------------|---------|--------------------------|
| 13880603 | 13880602 | | ALL | Waiver alt to Drawing |
| 35351681 | 35351294 | | ALL | UNOFFICIAL - OEM |
| 15280276 | 15280683 | | ALL | Waiver alt to Data/Label |
| 34182367 | 34182366 | | ALL | Waiver alt to BOM |
| 15281034 | 15280867 | | ALL | Waiver alt to Data |
| 15780058 | 15780055 | | ALL | Waiver alt to BOM Waiver |
| 15280915 | 15280796 | | ALL | Waiver alt to Option ID |
| 12880220 | 12880262 | | ALL | Waiver alt to BOM |
| 12780062 | 12780108 | | ALL | Waiver alt to BOM |
| 15280968 | 15280966 | | ALL | Waiver alt to Data |
| 31180447 | 31180406 | | ALL | Waiver alt to BOM |
| 33880714 | 33880554 | | ALL | Low Leakage DRG DRG |
| 10780138 | 10780074 | | ALL | CWTRC alt to VDS |
| 10780139 | 10780075 | | ALL | CWTRC alt to VDS |

BOM Configuration

SYNC_MASTER=DDR SYNC_DATE=12/18/2008

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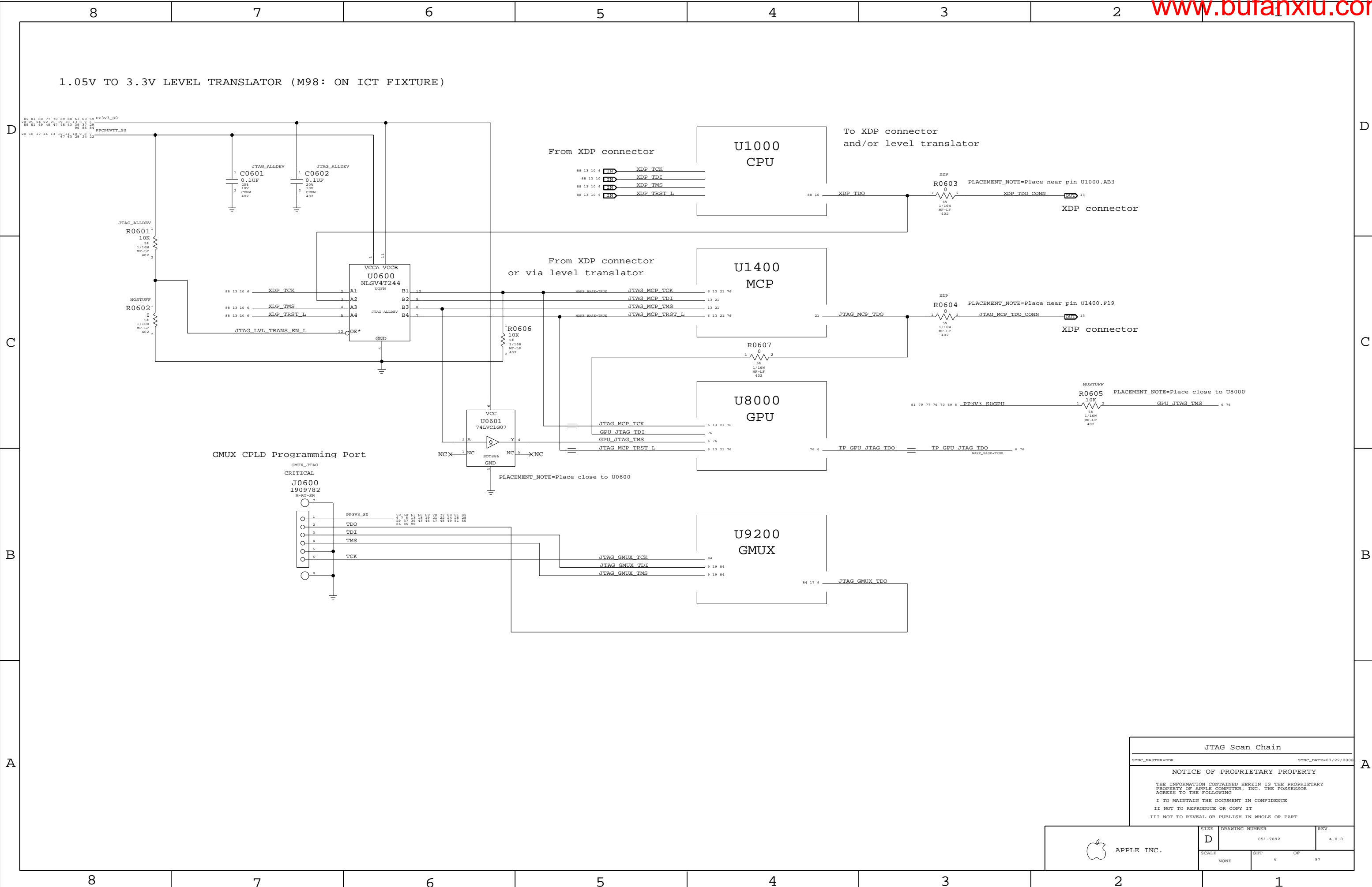
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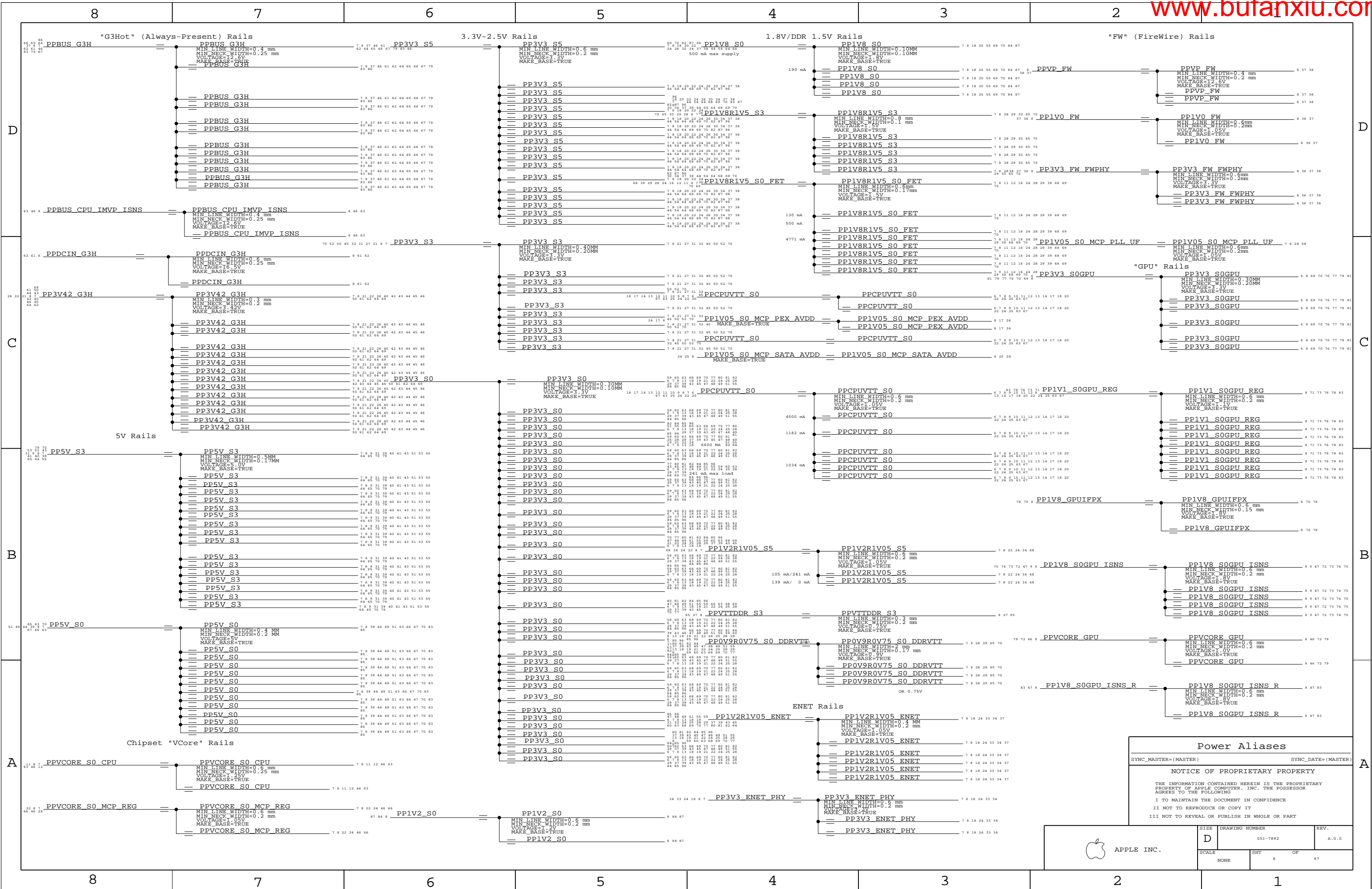
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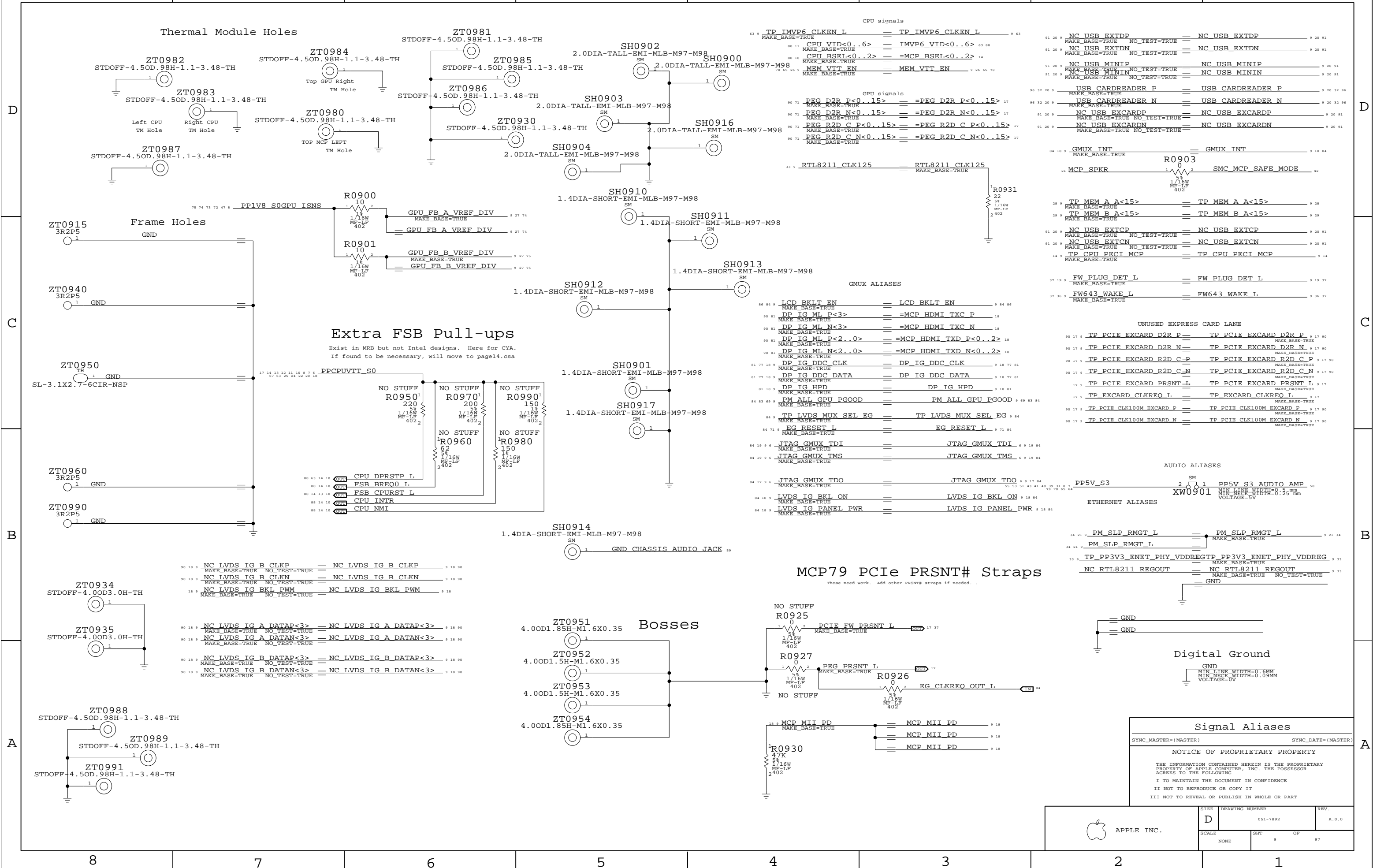
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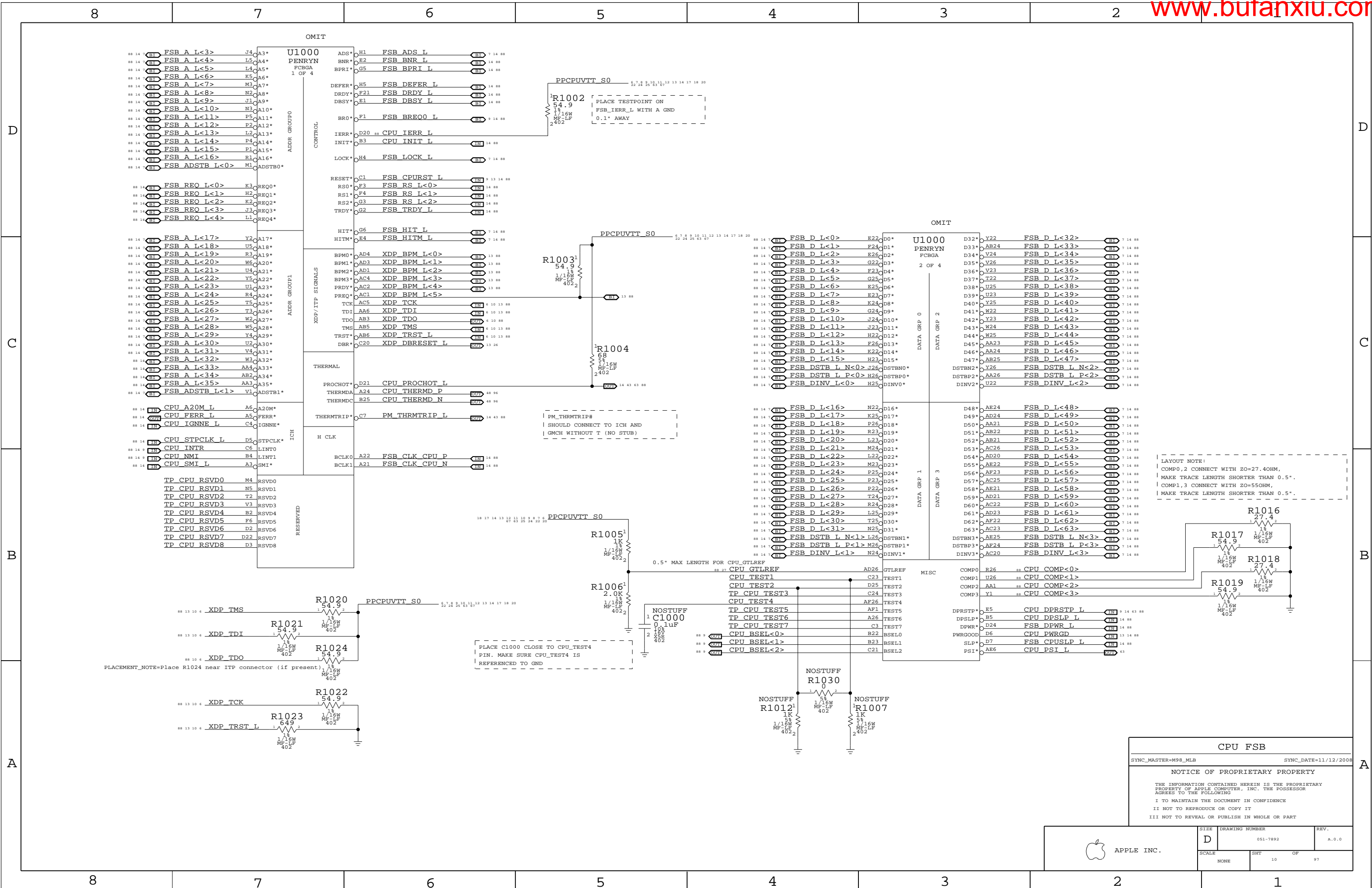
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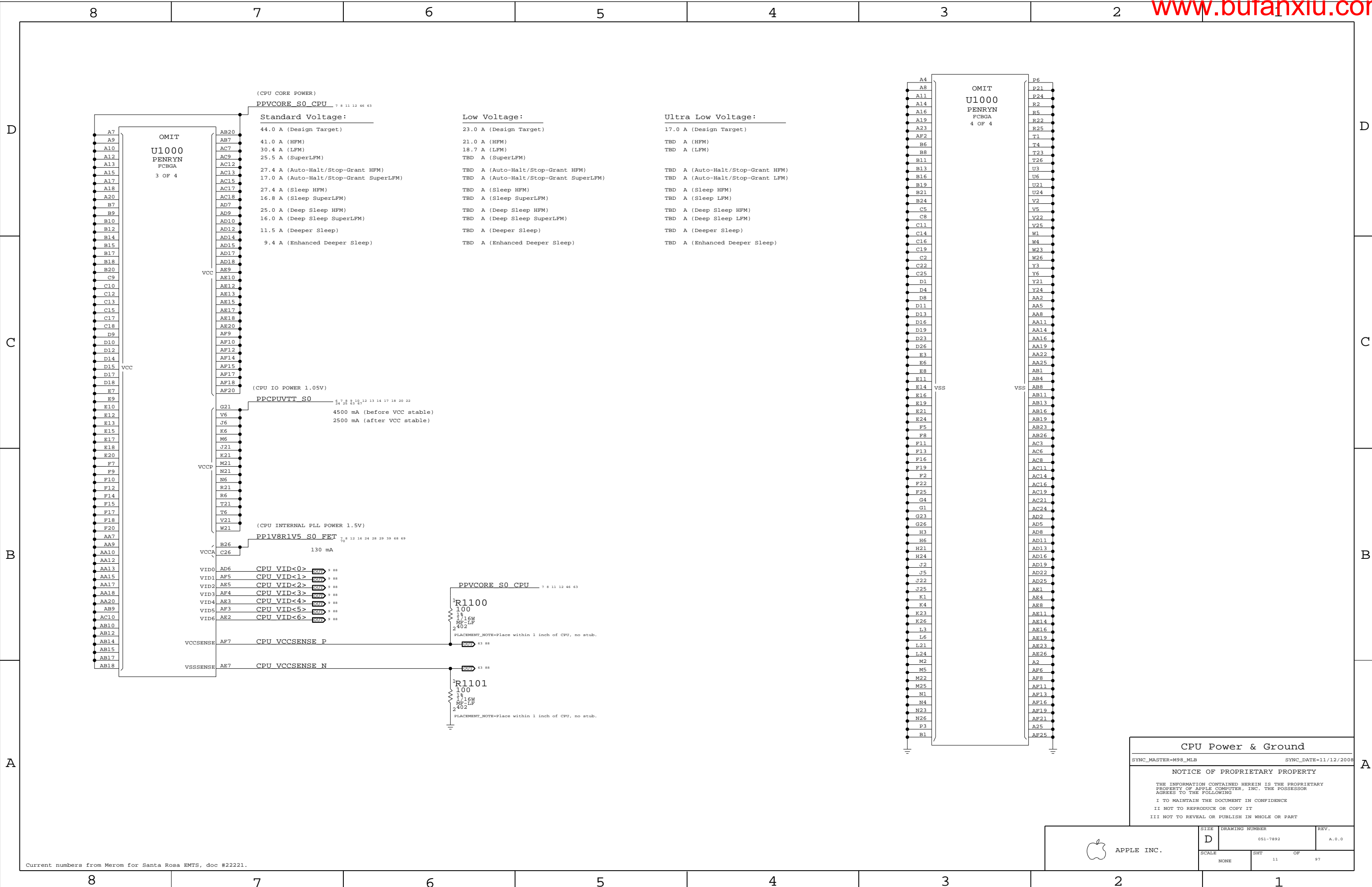
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CPU Power & Ground

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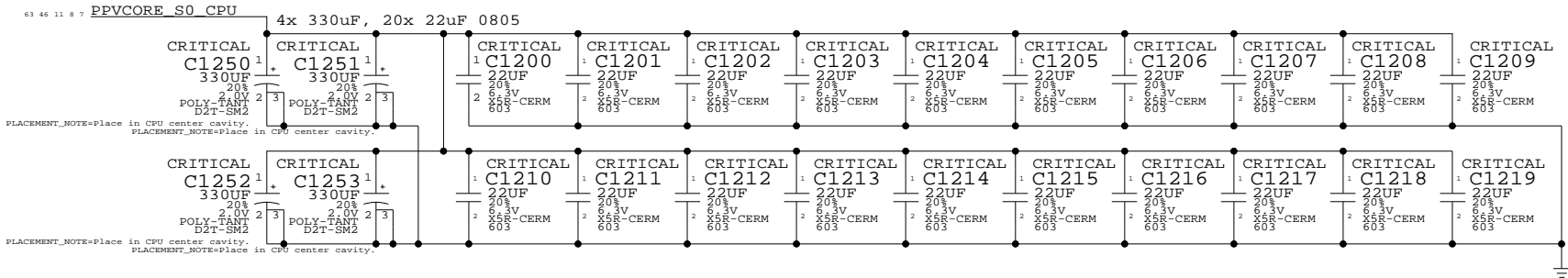
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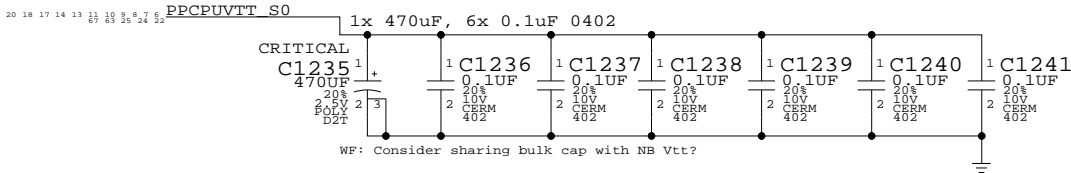
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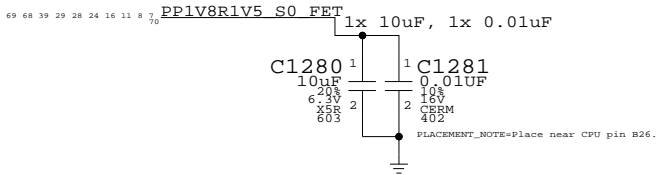
CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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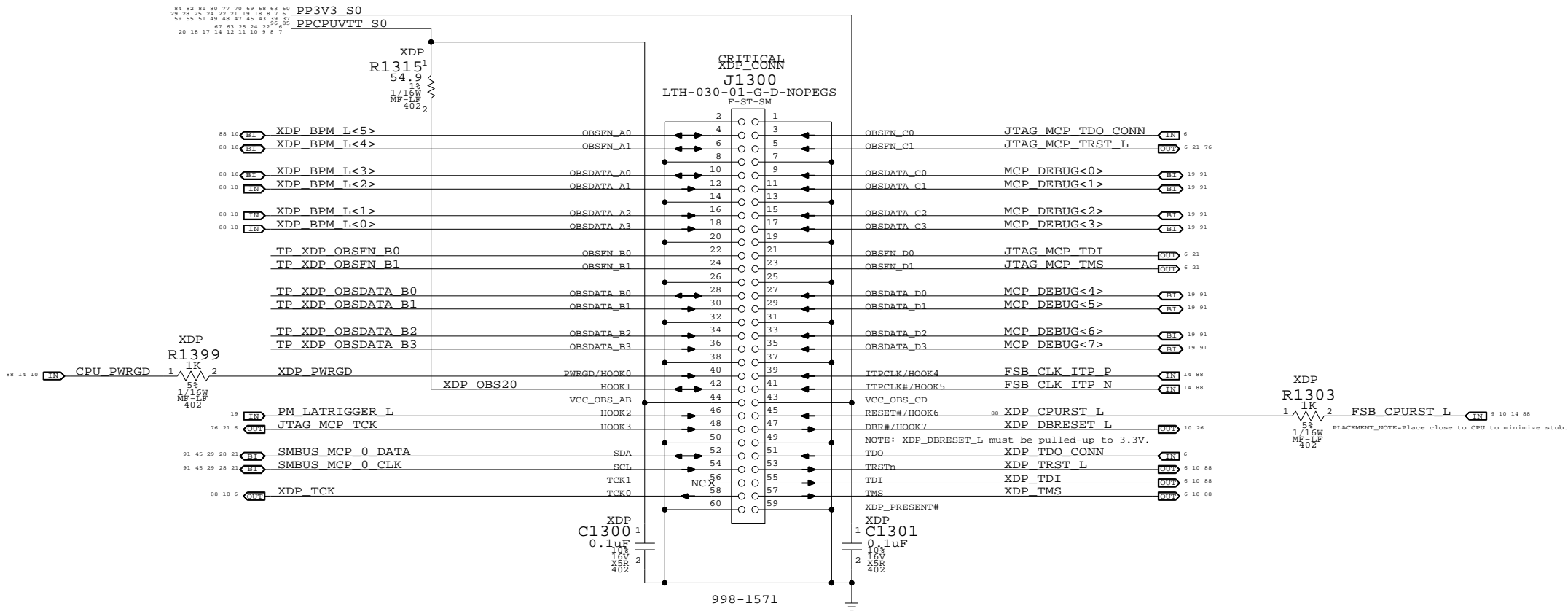
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97

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module
Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (MiniXDP)

SYNC_MASTER=M98_MLB SYNC_DATE=11/12/2008

NOTICE OF PROPRIETARY PROPERTY

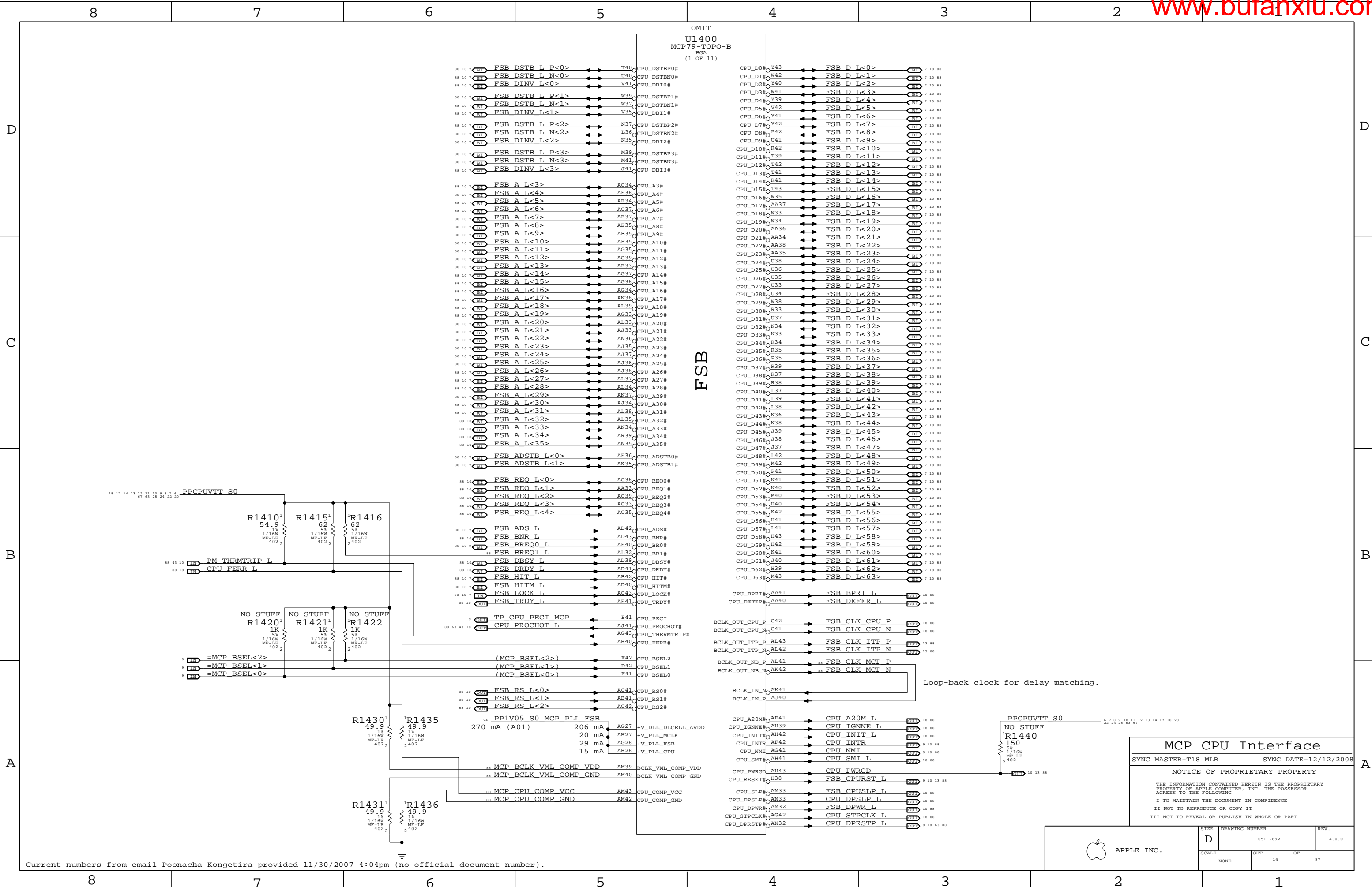
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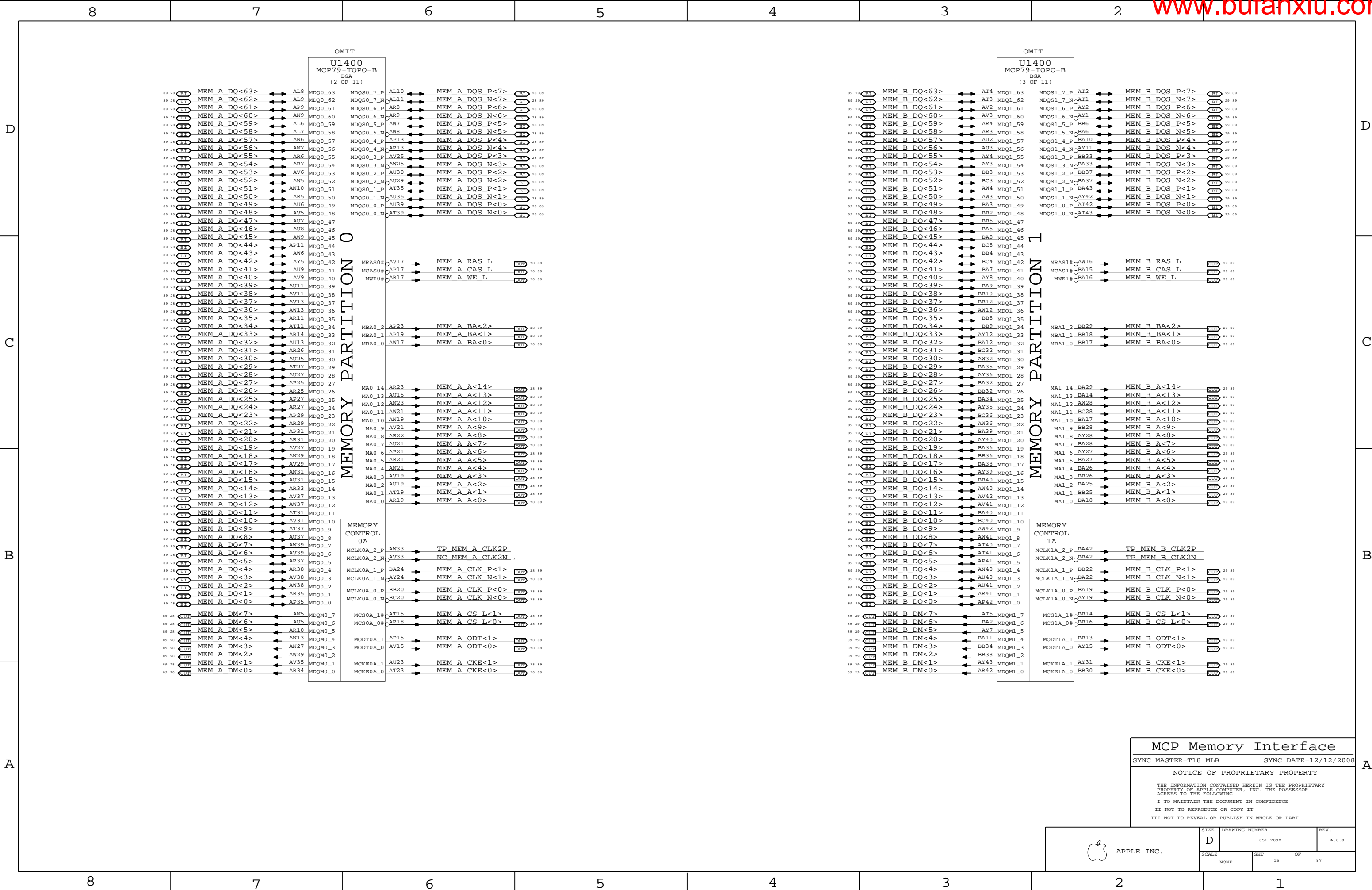
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| | D | 051-7892 | A.0.0 |
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| NONE | | 13 | 97 |





MCP Memory Interface

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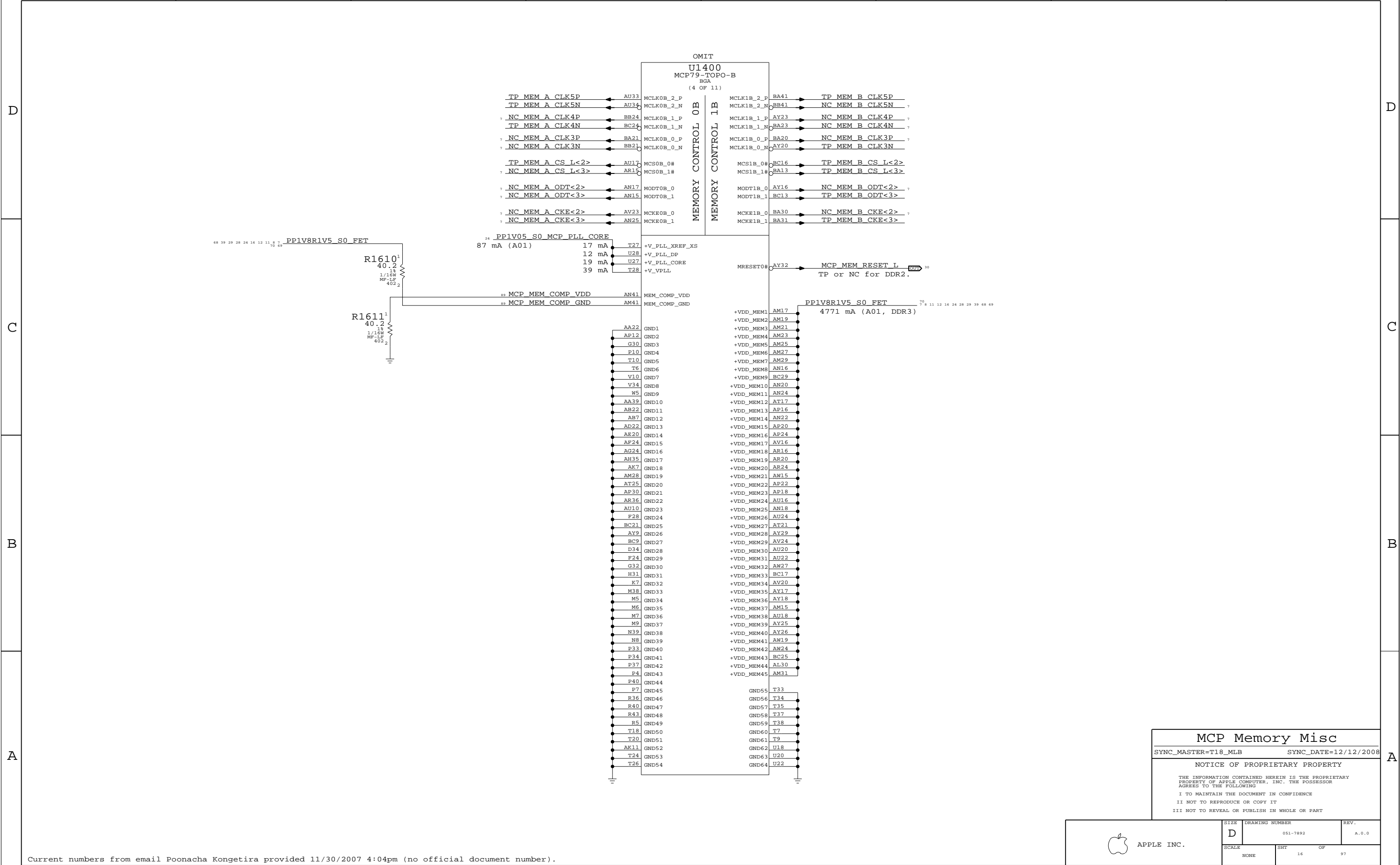
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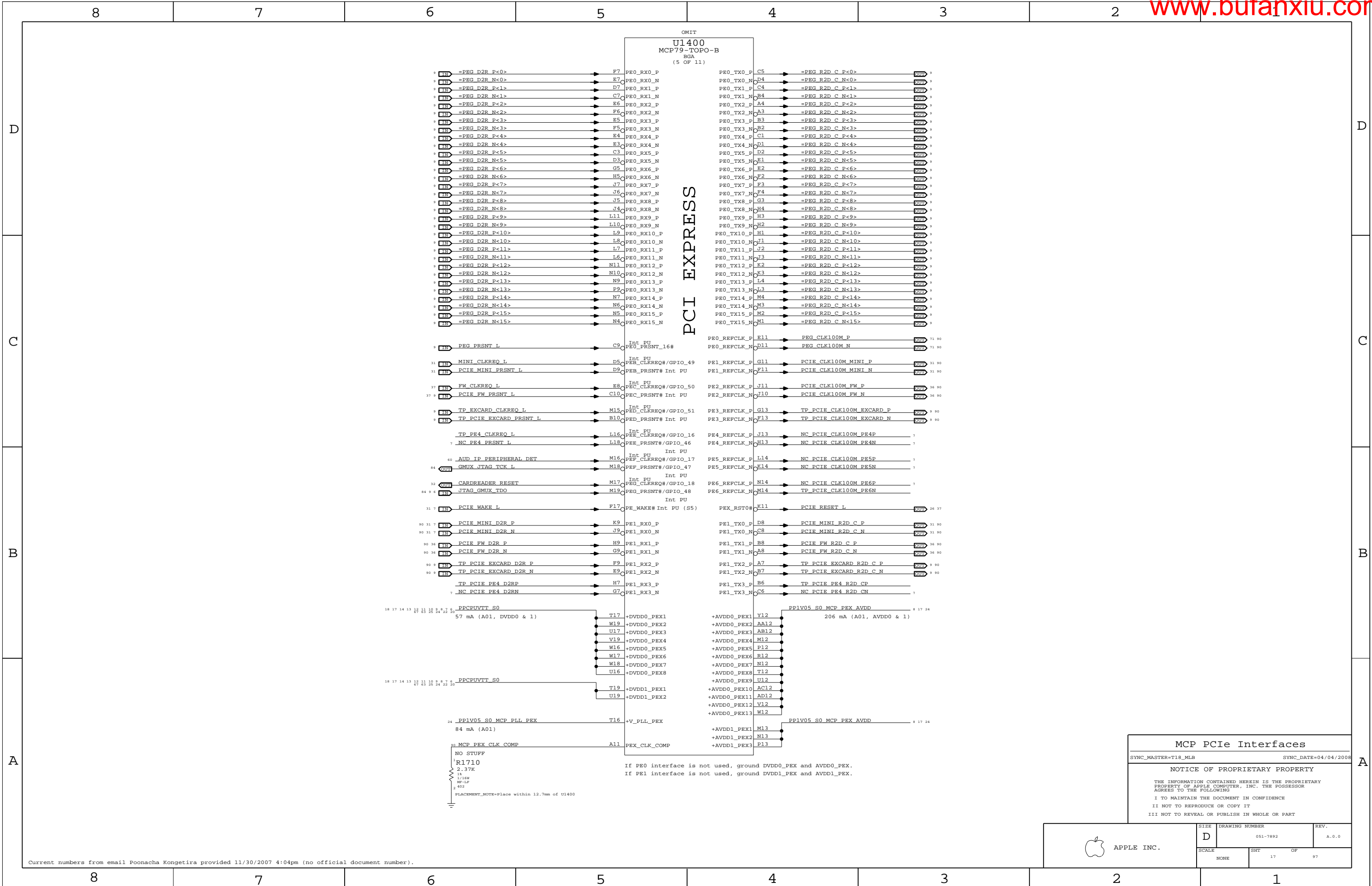
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MCP PCIe Interfaces

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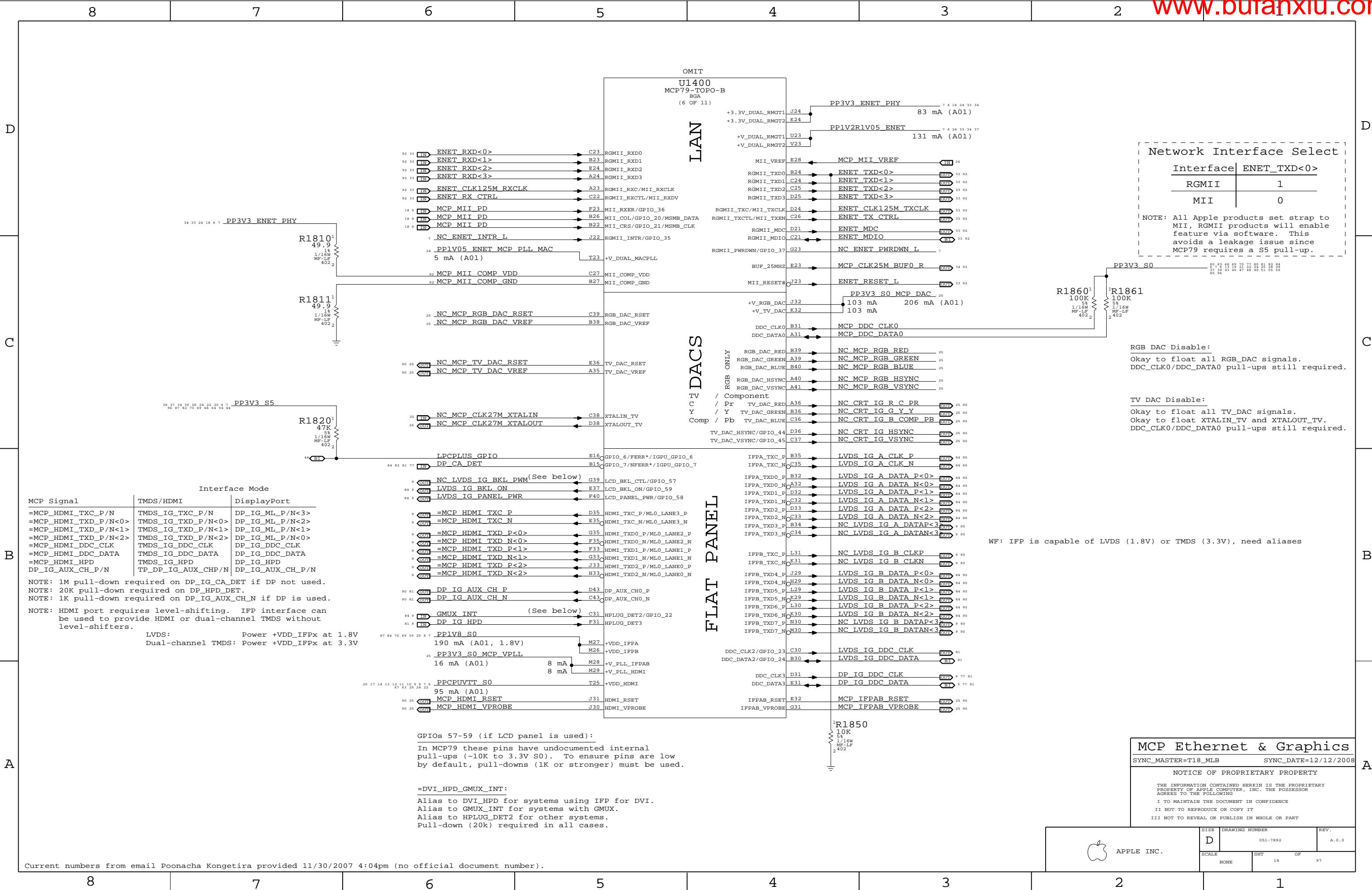
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SIZE D DRAWING NUMBER 051-7892 REV. A.0.0

SCALE NONE SHT 17 OF 97



| Network Interface Select | |
|--------------------------|-------------|
| Interface | ENET_TXD<0> |
| RGMII | 1 |
| MII | 0 |

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:
Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:
Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

MCP Ethernet & Graphics

SYNC_MASTER=T18_MLB

SYNC_DATE=12/12/2008

NOTICE OF PROPRIETARY PROPERTY

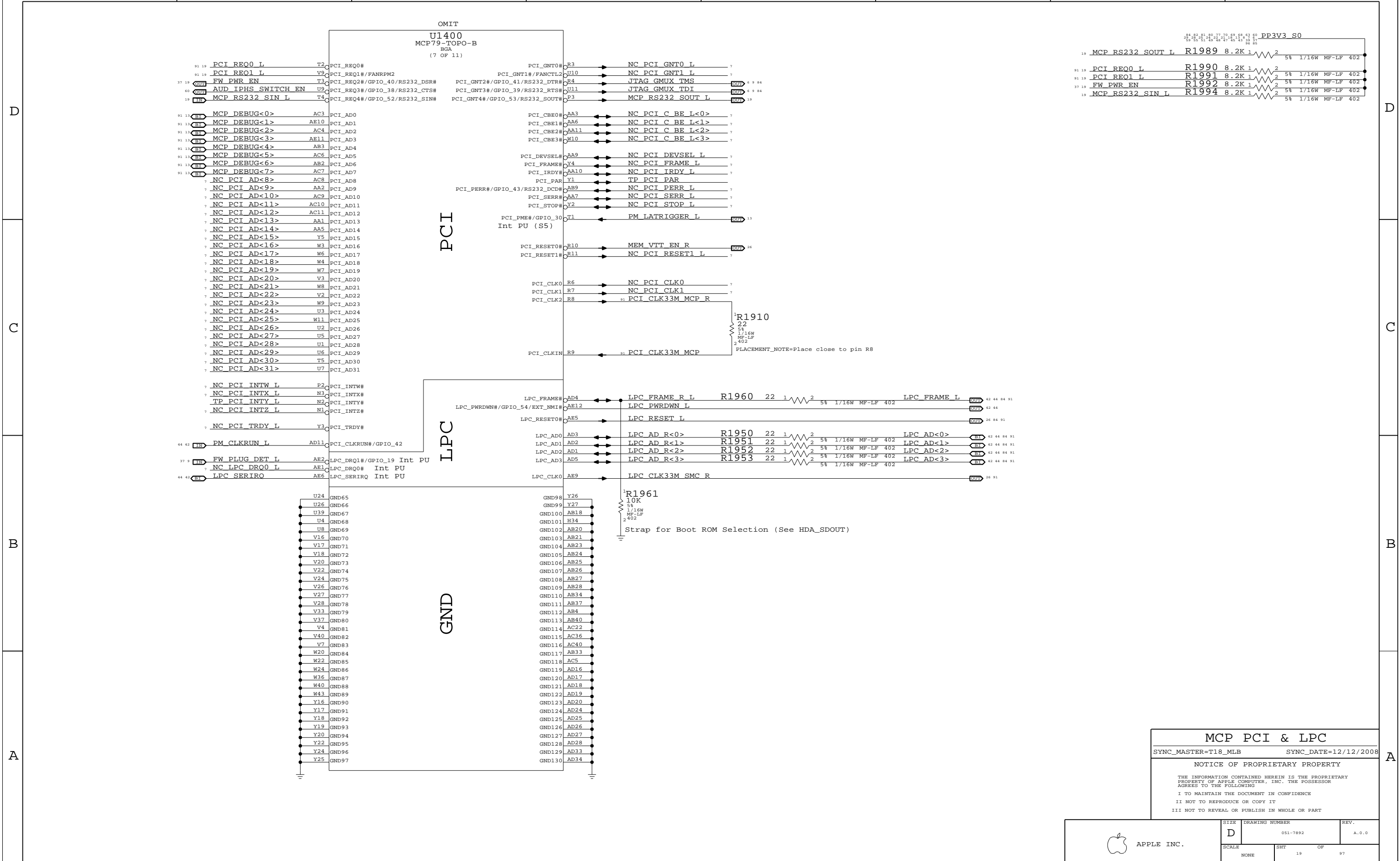
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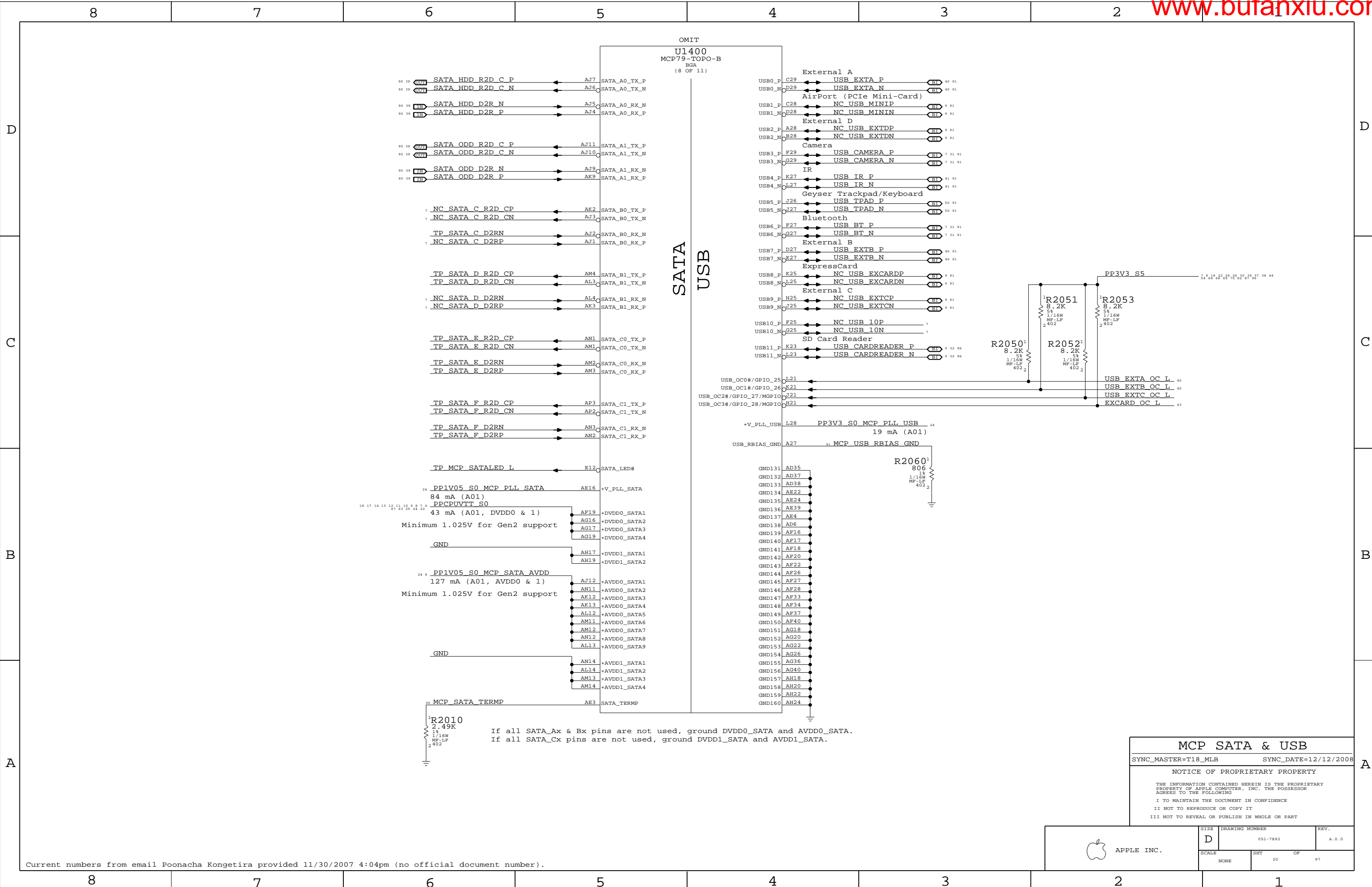
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| APPLE INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-7892 | A.0.0 |
| SCALE | | SHT | OF |
| NONE | | 18 | 97 |





If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

MCP SATA & USB

SYNC_MASTER=T18_MLB

SYNC_DATE=12/12/2008

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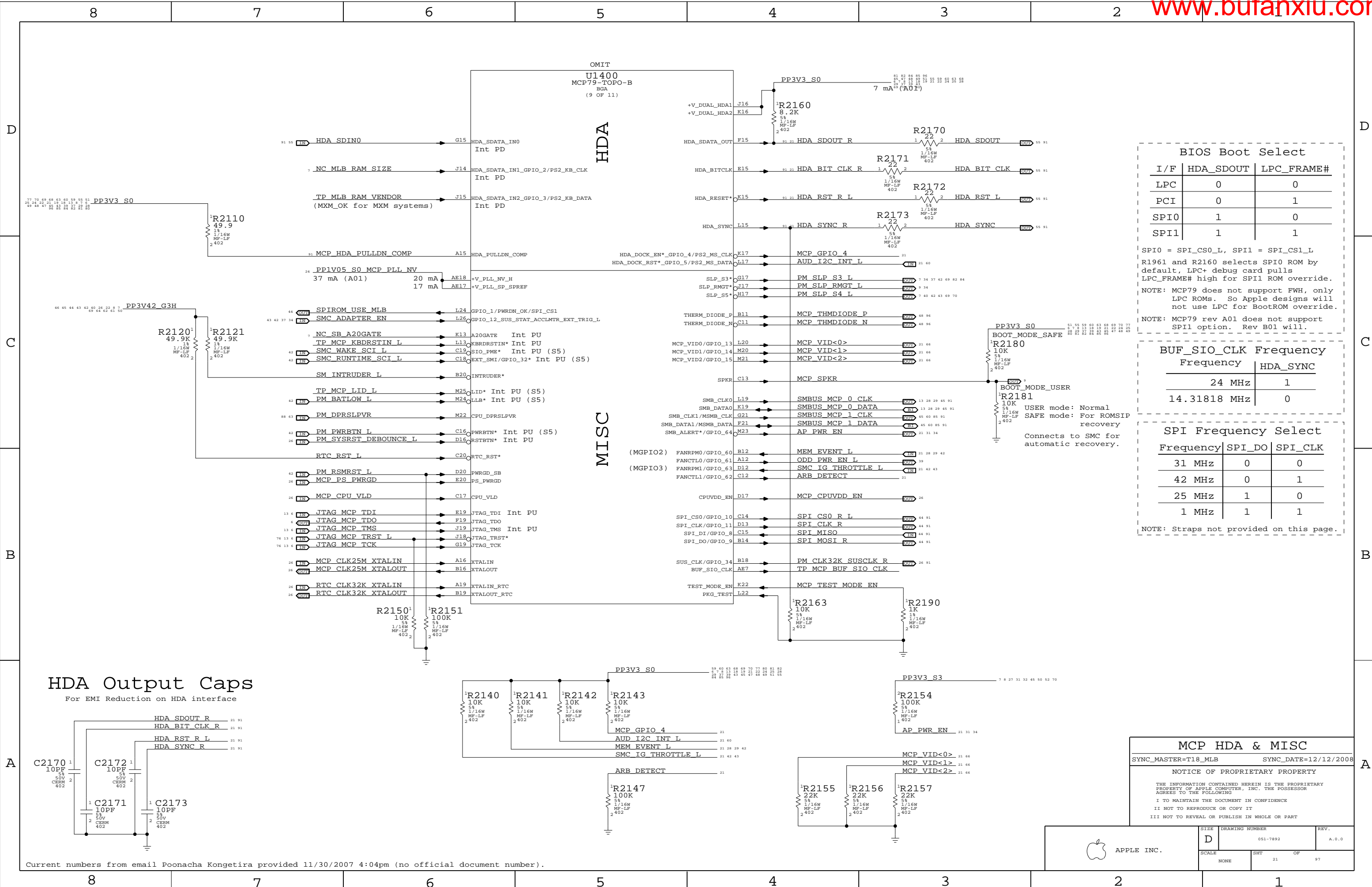
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| | D | 051-7892 | A.0.0 |
| SCALE | SHT | OF | |
| NONE | 20 | 97 | |



MCP HDA & MISC

SYNC_MASTER=T18_MLB

SYNC_DATE=12/12/2008

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APPLE INC.

SIZE D

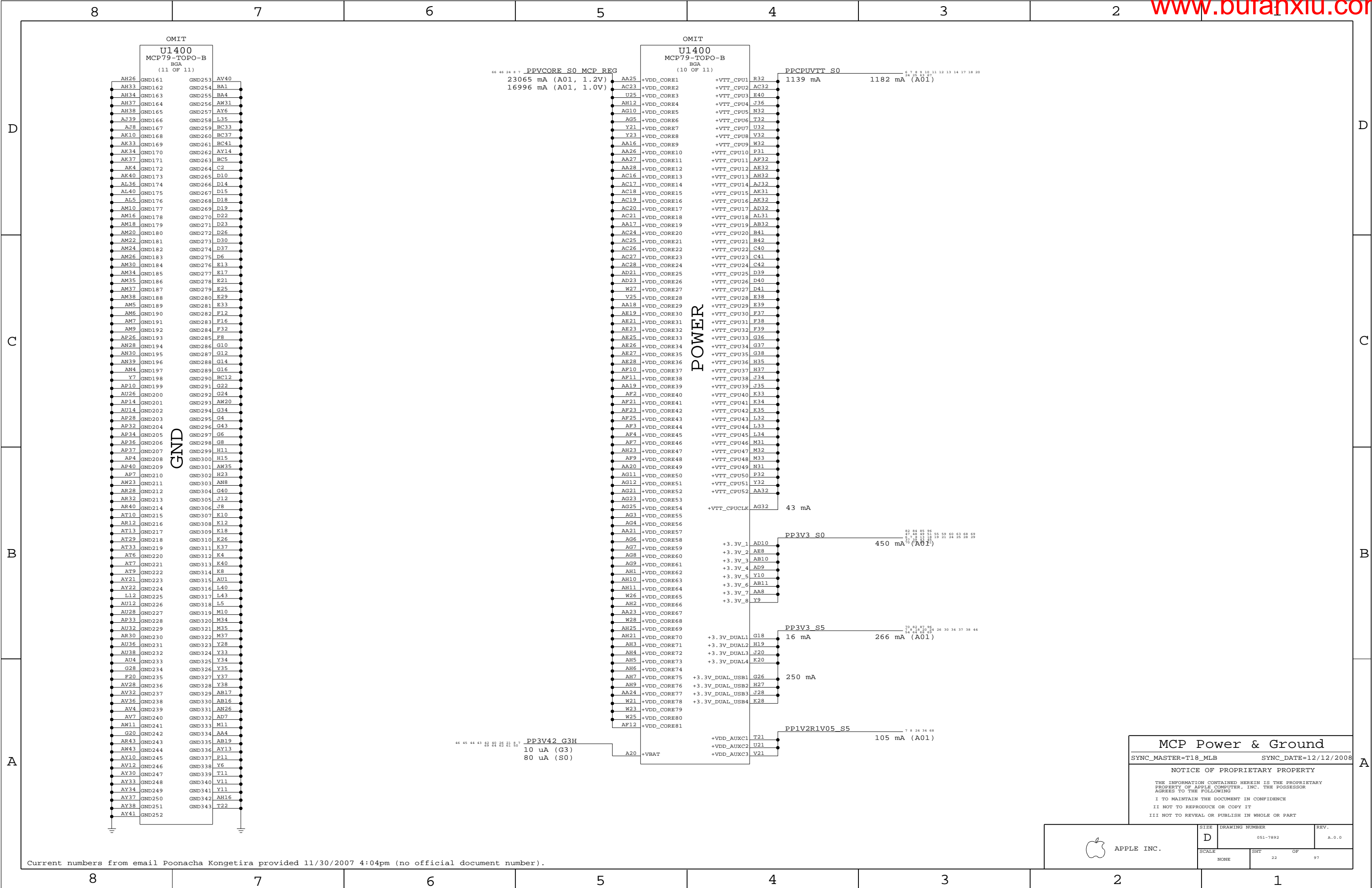
SCALE NONE

DRAWING NUMBER 051-7892

SHT 21

OF 97

REV. A.0.0



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Power & Ground

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

NOTICE OF PROPRIETARY PROPERTY

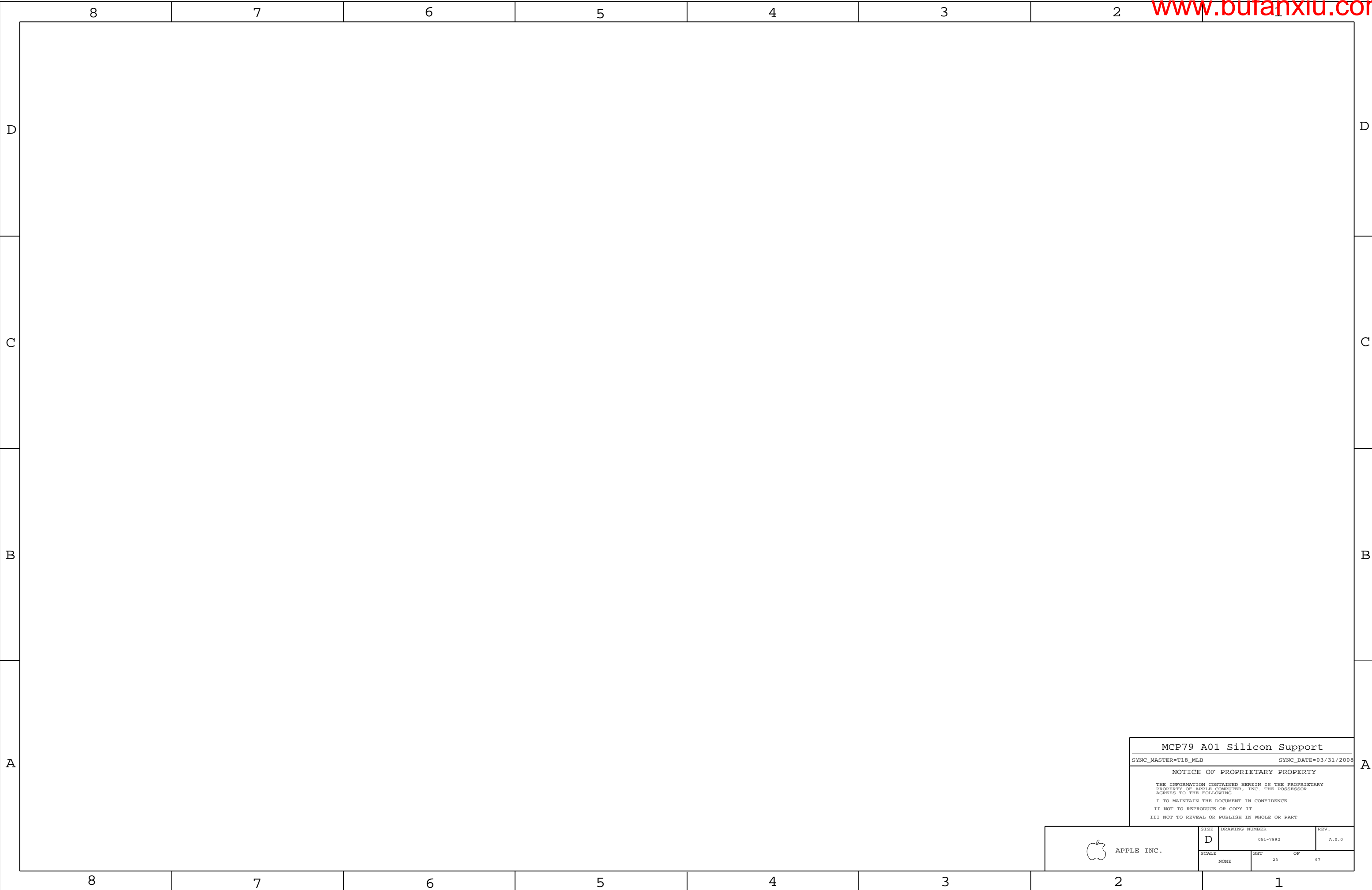
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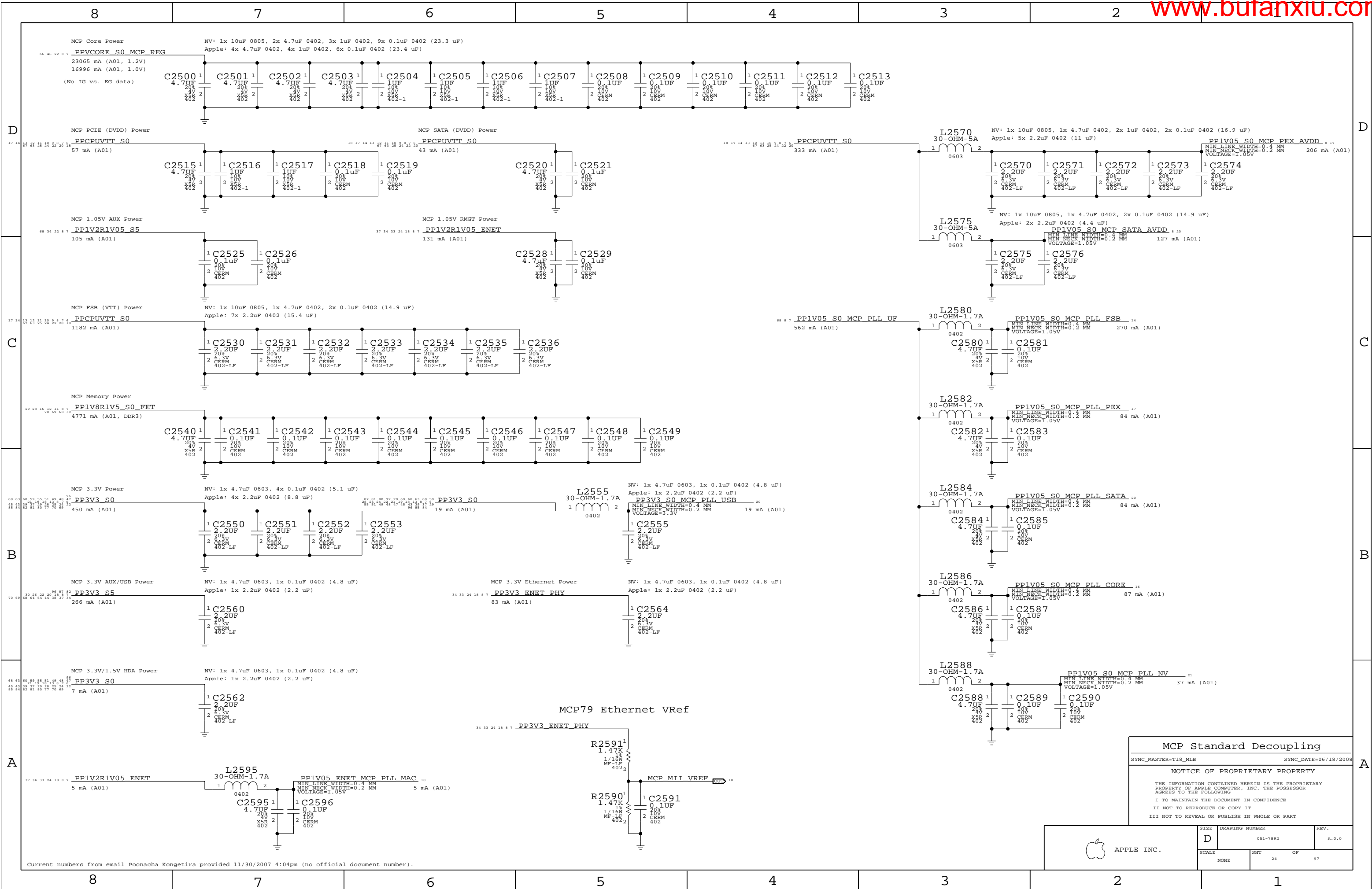
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| APPLE INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-7892 | A.0.0 |
| | SCALE | SHT | OF |
| | NONE | 22 | 97 |



| | | | |
|--|---------------|----------------------------|---------------|
| MCP79 A01 Silicon Support | | | |
| SYNC_MASTER=T18_MLB | | SYNC_DATE=03/31/2008 | |
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| | SCALE NONE | SHT 23 OF 97 | |



MCP Standard Decoupling

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

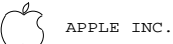
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|-------|----------------|-------|
| D | 051-7892 | A.0.0 |
| SCALE | SHT | OF |
| NONE | 24 | 97 |

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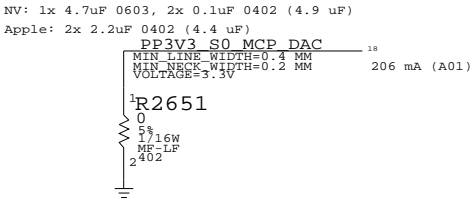
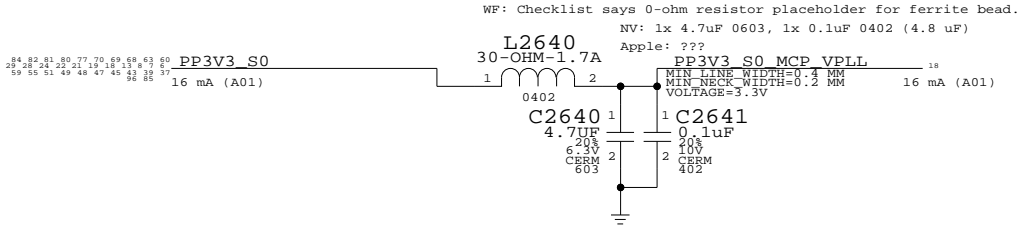
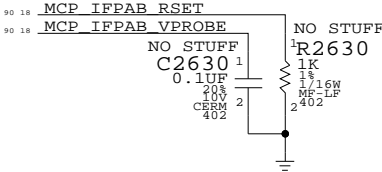
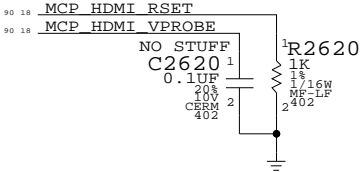
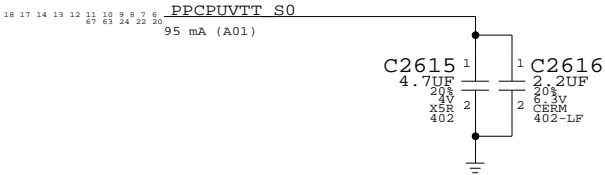
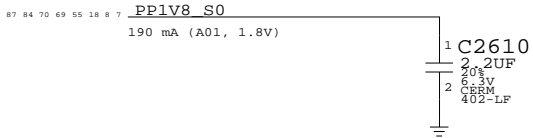
C

B

A

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)



| | | | | |
|----------|-----------------------|----|-----------------------------|----------|
| 25 18 | NC MCP RGB RED | == | NC MCP RGB RED | 18 25 |
| 25 18 | NC MCP RGB GREEN | == | MAKE_BASE=TRUE NO_TEST=TRUE | 18 25 |
| 25 18 | NC MCP RGB BLUE | == | MAKE_BASE=TRUE NO_TEST=TRUE | 18 25 |
| 25 18 | NC MCP RGB HSYNC | == | NC MCP RGB HSYNC | 18 25 |
| 25 18 | NC MCP RGB VSYNC | == | MAKE_BASE=TRUE NO_TEST=TRUE | 18 25 |
| 90 25 18 | NC CRT IG R C PR | == | NC CRT IG R C PR | 18 25 90 |
| 90 25 18 | NC CRT IG G Y Y | == | MAKE_BASE=TRUE NO_TEST=TRUE | 18 25 90 |
| 90 25 18 | NC CRT IG B COMP PB | == | MAKE_BASE=TRUE NO_TEST=TRUE | 18 25 90 |
| 90 25 18 | NC CRT IG HSYNC | == | NC CRT IG HSYNC | 18 25 90 |
| 90 25 18 | NC CRT IG VSYNC | == | MAKE_BASE=TRUE NO_TEST=TRUE | 18 25 90 |
| 25 18 | NC MCP RGB DAC RSET | == | NC MCP RGB DAC RSET | 18 25 |
| 25 18 | NC MCP RGB DAC VREF | == | MAKE_BASE=TRUE NO_TEST=TRUE | 18 25 |
| 90 25 18 | NC MCP TV DAC RSET | == | NC MCP TV DAC RSET | 18 25 90 |
| 90 25 18 | NC MCP TV DAC VREF | == | MAKE_BASE=TRUE NO_TEST=TRUE | 18 25 90 |
| 25 18 | NC MCP CLK27M XTALIN | == | NC MCP CLK27M XTALIN | 18 25 |
| 25 18 | NC MCP CLK27M XTALOUT | == | MAKE_BASE=TRUE NO_TEST=TRUE | 18 25 |

MCP Graphics Support

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008

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APPLE INC.

SIZE

D

DRAWING NUMBER

051-7892

REV.

A.0.0

SCALE

NONE

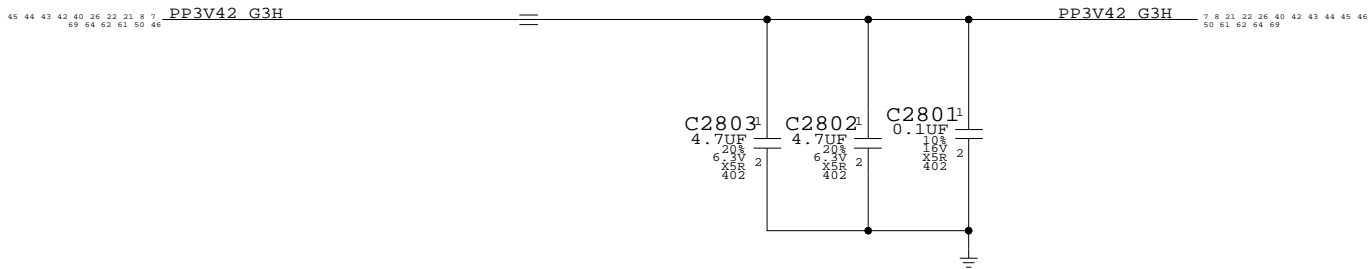
SHT

25

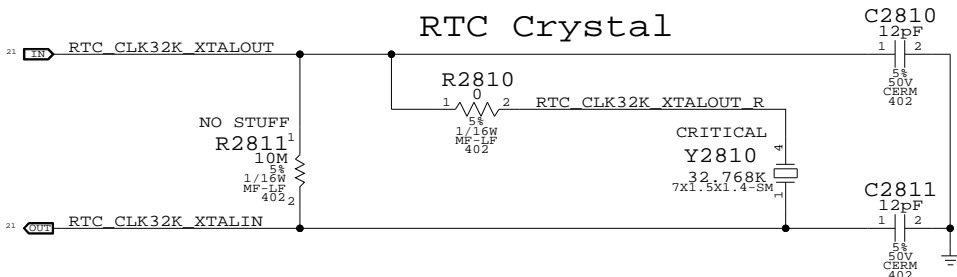
OF

97

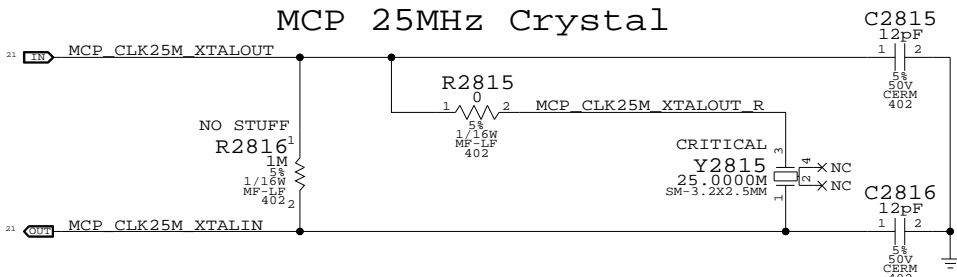
RTC Power Sources



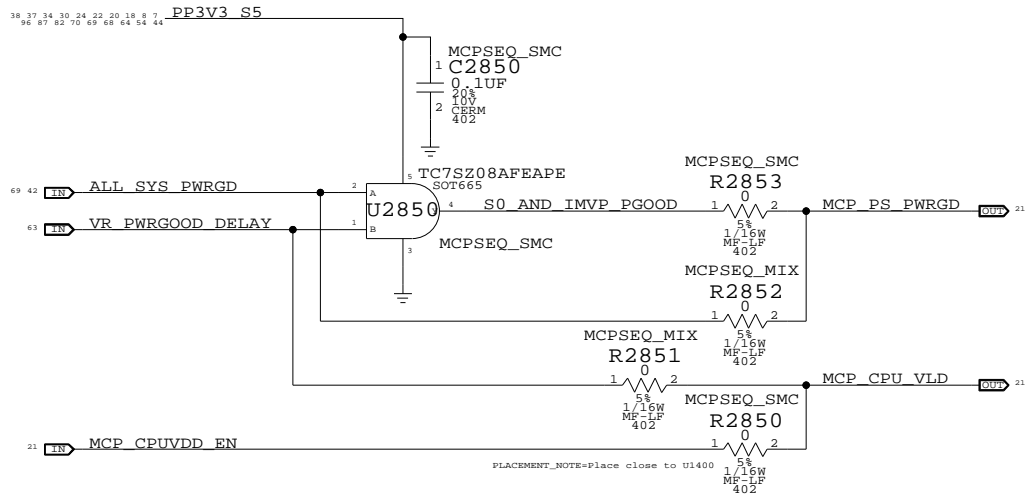
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

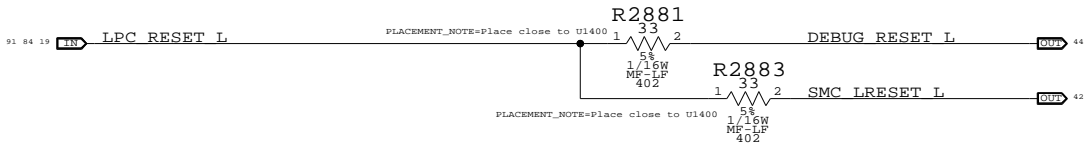
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

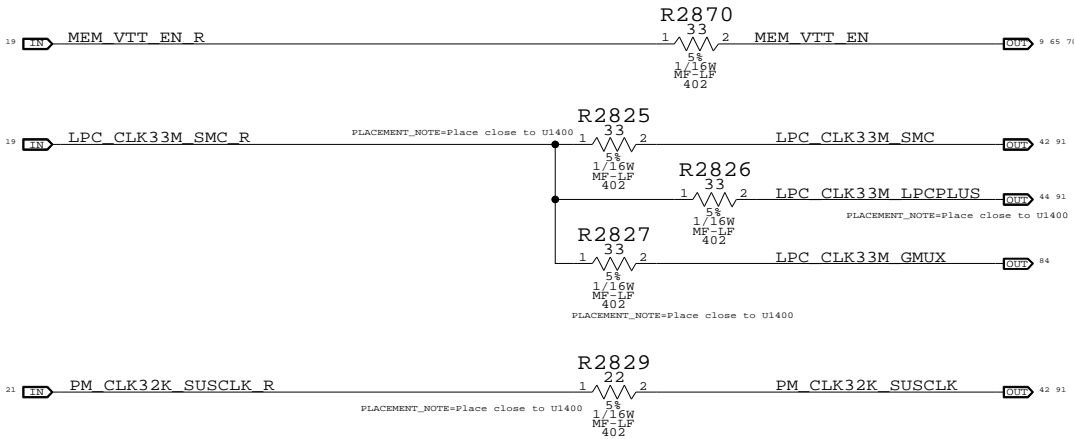
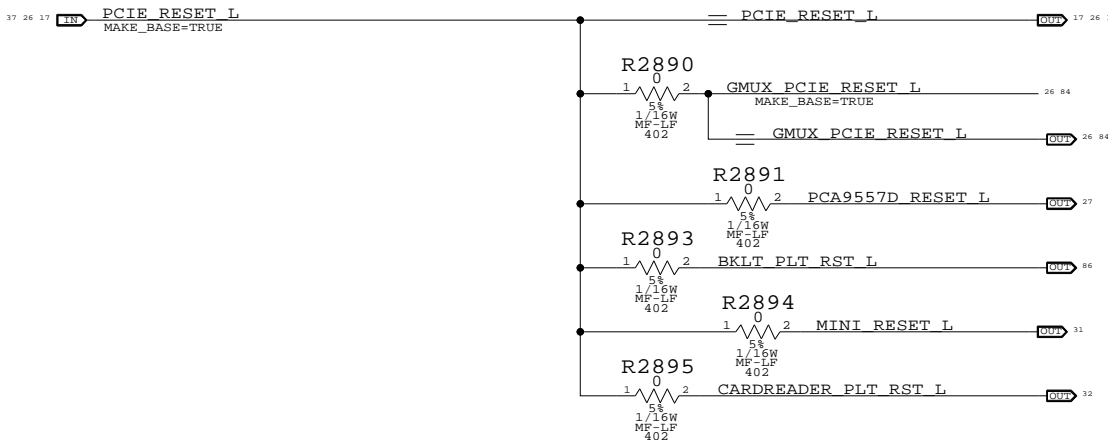
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

Platform Reset Connections

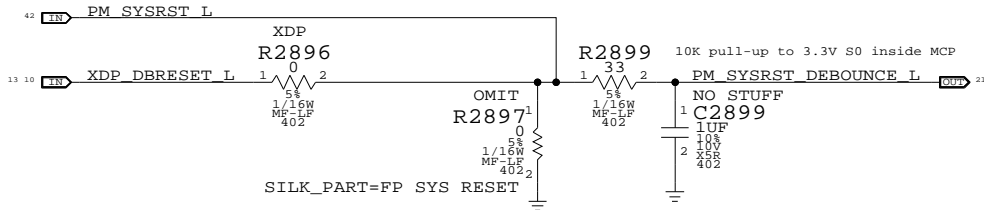
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



Reset Button



SB Misc

SYNC_MASTER=DDR SYNC_DATE=12/15/2008

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|-------|----------------|-------|
| D | 051-7892 | A.0.0 |
| SCALE | SHT | OF |
| NONE | 26 | 97 |

Page Notes

Power aliases required by this page:

- PP3V3_S3_VREFMRGN
- PP3V3_S5_VREFMRGN
- PPVT_S3_DDR_BUF

Signal aliases required by this page:

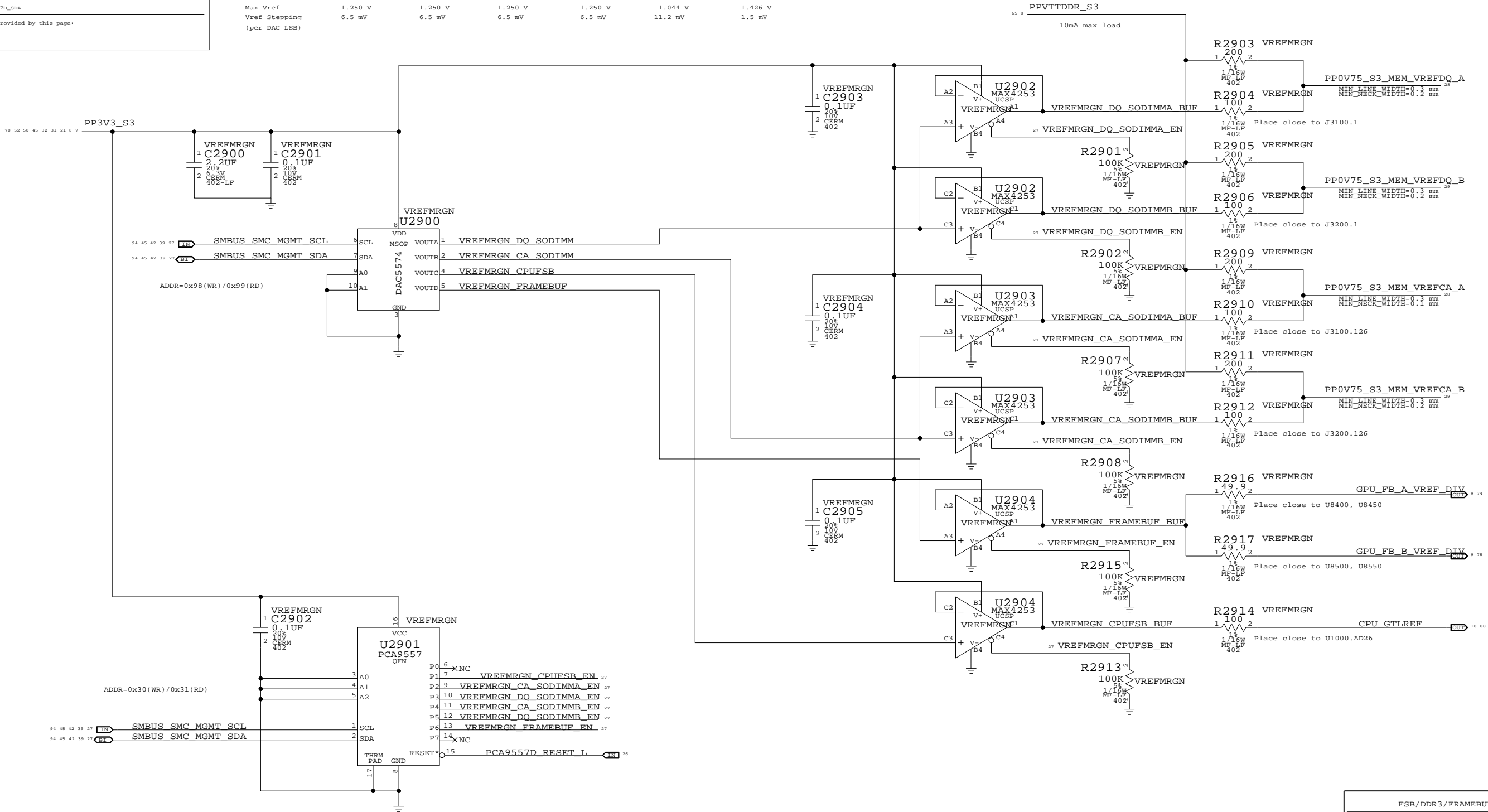
- I2C_VREFDACS_SCL
- I2C_VREFDACS_SDA
- I2C_PCA9557D_SCL
- I2C_PCA9557D_SDA

BOM options provided by this page:

- VREFMRGN
- NO_VREFMRGN

| | MEM A VREF DQ | | MEM A VREF CA | | MEM B VREF DQ | | MEM B VREF CA | | CPU FSB VREF | FRAME BUFFER VREF |
|-----------------------------|---------------|----------|---------------|----------|---------------|----------|---------------|-----------|--------------|-------------------|
| DAC channel | A | B | A | B | A | B | C | D | | |
| Min DAC code | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | | |
| Max DAC code | 0x87 | 0x87 | 0x87 | 0x87 | 0x87 | 0x87 | 0x55 | 0xFF | | |
| Max sink I | -3.75 mA | -3.75 mA | -3.75 mA | -3.75 mA | -3.75 mA | -3.75 mA | -0.91 mA | -59.04 mA | | |
| Max source I | 5 mA | 5 mA | 5 mA | 5 mA | 5 mA | 5 mA | 0.52 mA | 51.15 mA | | |
| Nominal Vref | 0.75 V | 0.75 V | 0.75 V | 0.75 V | 0.75 V | 0.75 V | 0.70 V | 1.248 V | | |
| Min Vref | 0.375 V | 0.375 V | 0.375 V | 0.375 V | 0.375 V | 0.375 V | 0.091 V | 1.042 V | | |
| Max Vref | 1.250 V | 1.250 V | 1.250 V | 1.250 V | 1.250 V | 1.250 V | 1.044 V | 1.426 V | | |
| Vref Stepping (per DAC LSB) | 6.5 mV | 6.5 mV | 6.5 mV | 6.5 mV | 6.5 mV | 6.5 mV | 11.2 mV | 1.5 mV | | |

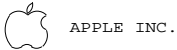
SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

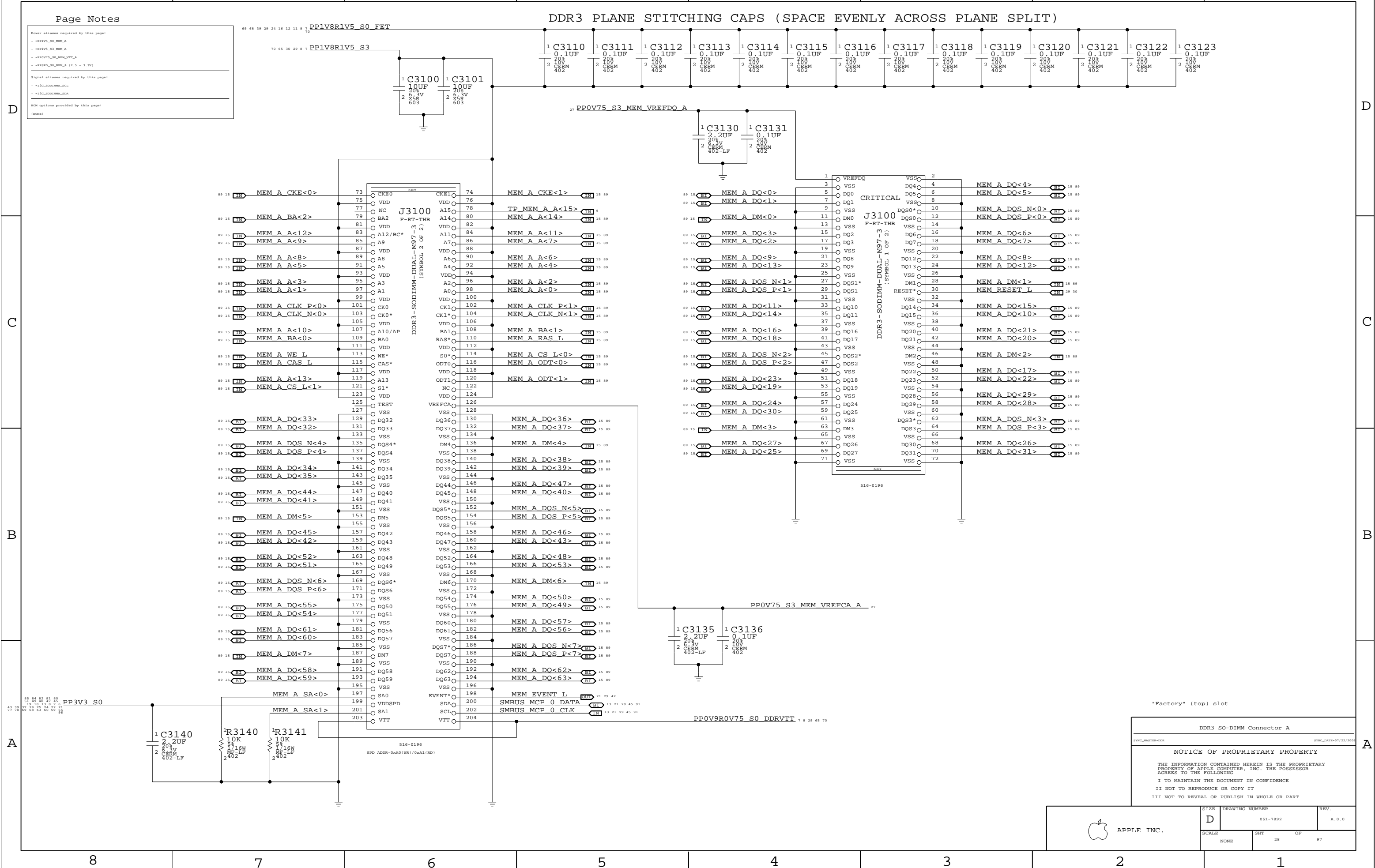
| PART NUMBER | QTY | DESCRIPTION | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|------------------------------|---------------|----------|-------------|
| 116S0004 | 1 | RES,MTL FILM,0,5%,0402,SM,LF | R2903 | CRITICAL | NO_VREFMRGN |
| 116S0004 | 1 | RES,MTL FILM,0,5%,0402,SM,LF | R2905 | CRITICAL | NO_VREFMRGN |
| 116S0004 | 1 | RES,MTL FILM,0,5%,0402,SM,LF | R2909 | CRITICAL | NO_VREFMRGN |
| 116S0004 | 1 | RES,MTL FILM,0,5%,0402,SM,LF | R2911 | CRITICAL | NO_VREFMRGN |

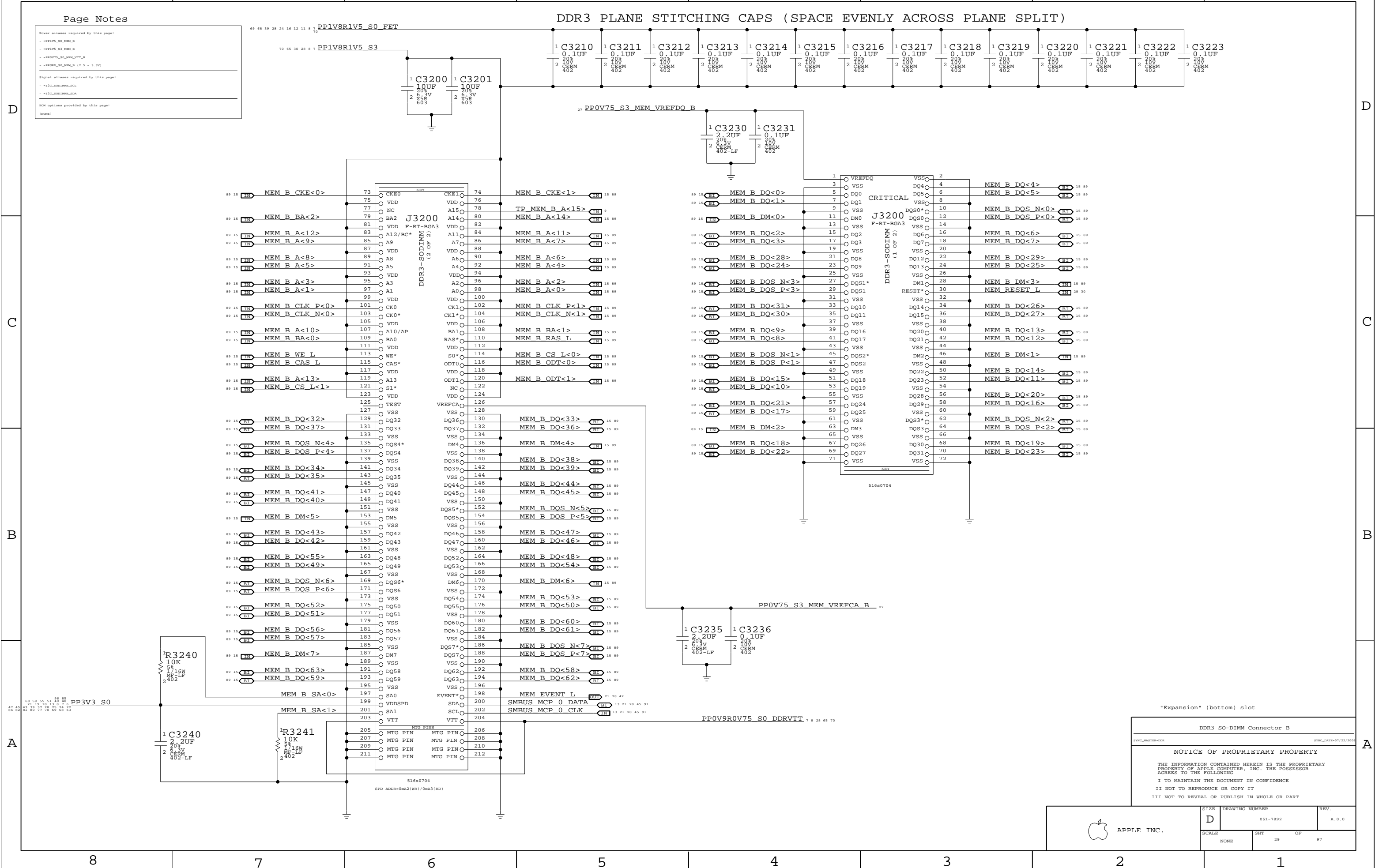
| FSB/DDR3/FRAMEBUF Vref Margining | | |
|--|--|----------------------|
| SYNC_MASTER=DDR | | SYNC_DATE=12/05/2008 |
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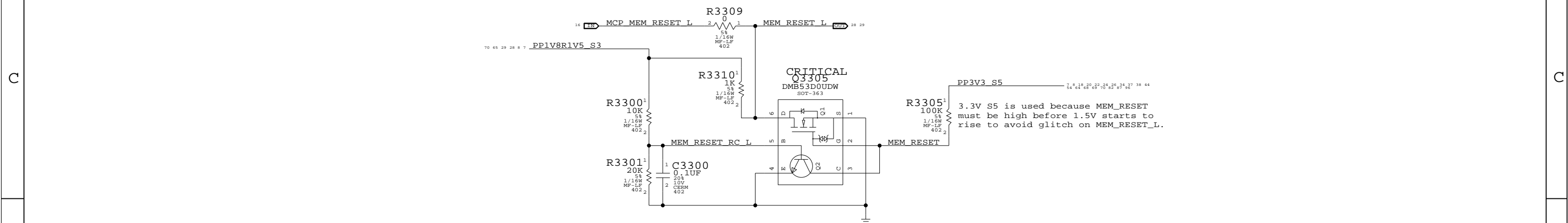
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|-------|----------------|-------|
| D | 051-7892 | A.0.0 |
| SCALE | SHT | OF |
| NONE | 27 | 97 |





DDR3 RESET Support
Required because MCP79 does not meet DDR3 spec power-up reset timing requirement.

| | |
|--|---|
| | Required because MCP79 does not meet DDR3 spec power-up reset timing requirement. |
|--|---|



| | | | |
|---|--|--|---|
| A | DDR3 Support | | Z |
| | SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008 | | |
| | | | |

| | |
|---------------------|----------------------|
| SYNC_MASTER=T18_MLB | SYNC_DATE=12/12/2008 |
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| D | 051-7892 | A.0.0 |

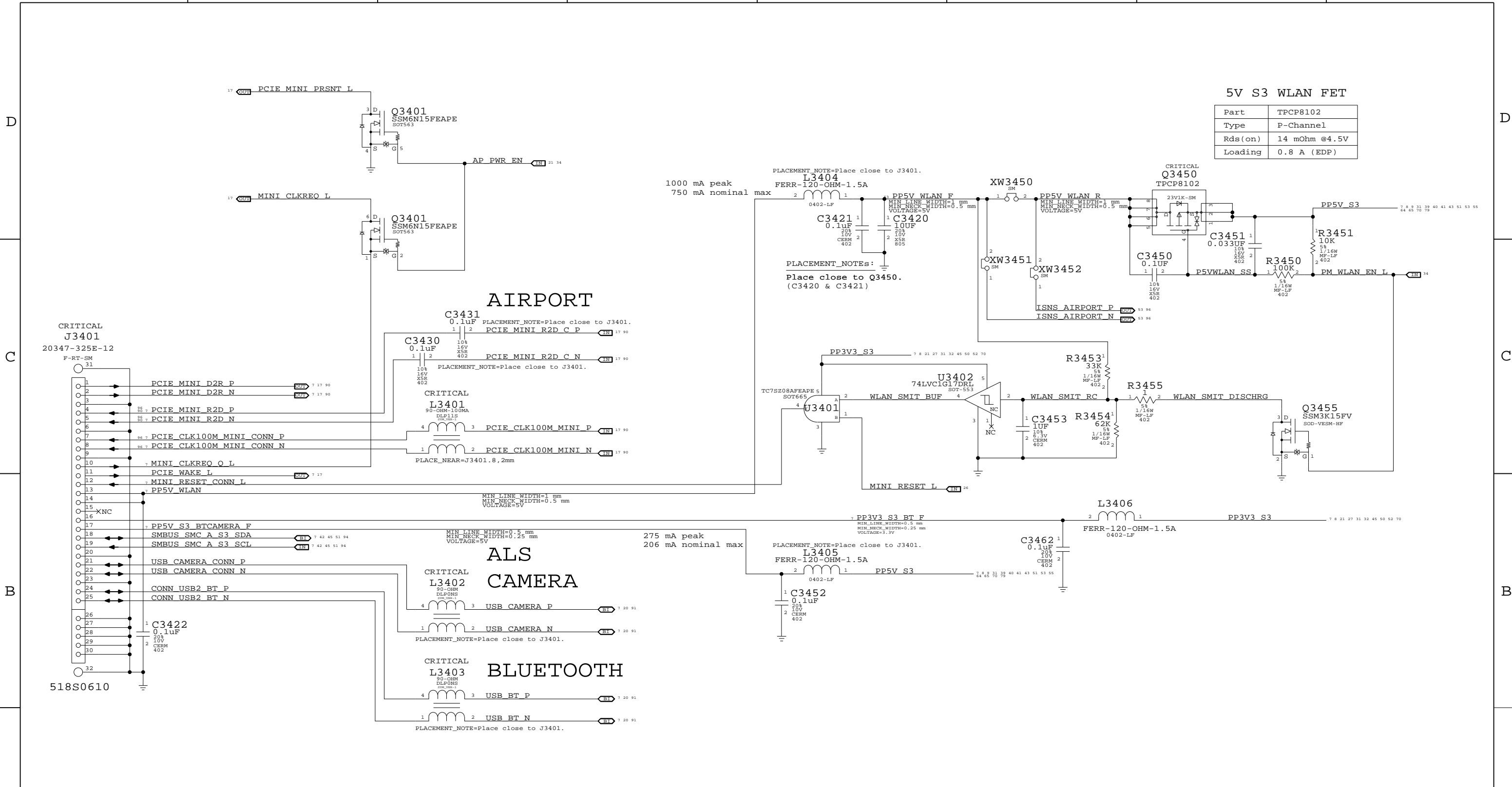
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| SCALE | SHT | OF |
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| | NONE | 30 | 97 |
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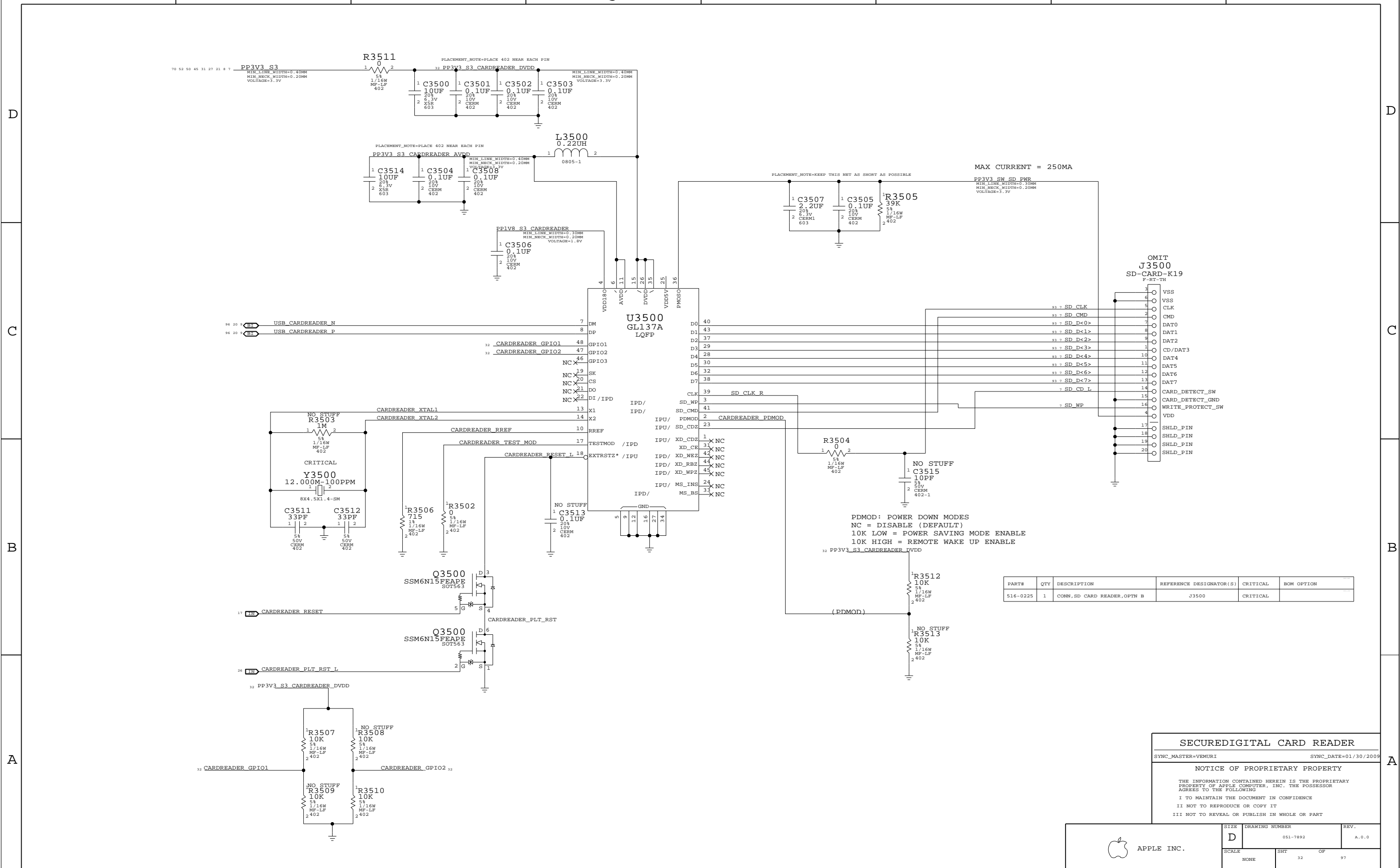
[illegible]

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|



| | |
|---------|---------------|
| Part | TPCP8102 |
| Type | P-Channel |
| Rds(on) | 14 mOhm @4.5V |
| Loading | 0.8 A (EDP) |

| | |
|---|----------------------|
| Right Clutch Connector | |
| SYNC_MASTER=MUXGFX | SYNC_DATE=12/08/2008 |
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| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|----------------------------|-------------------------|----------|------------|
| 516-0225 | 1 | CONN,SD CARD READER,OPTN B | J3500 | CRITICAL | |

SECUREDIGITAL CARD READER

SYNC_MASTER=VEMURI SYNC_DATE=01/30/2009

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APPLE INC.

SIZE
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DRAWING NUMBER

EV.

SCALE

SHT

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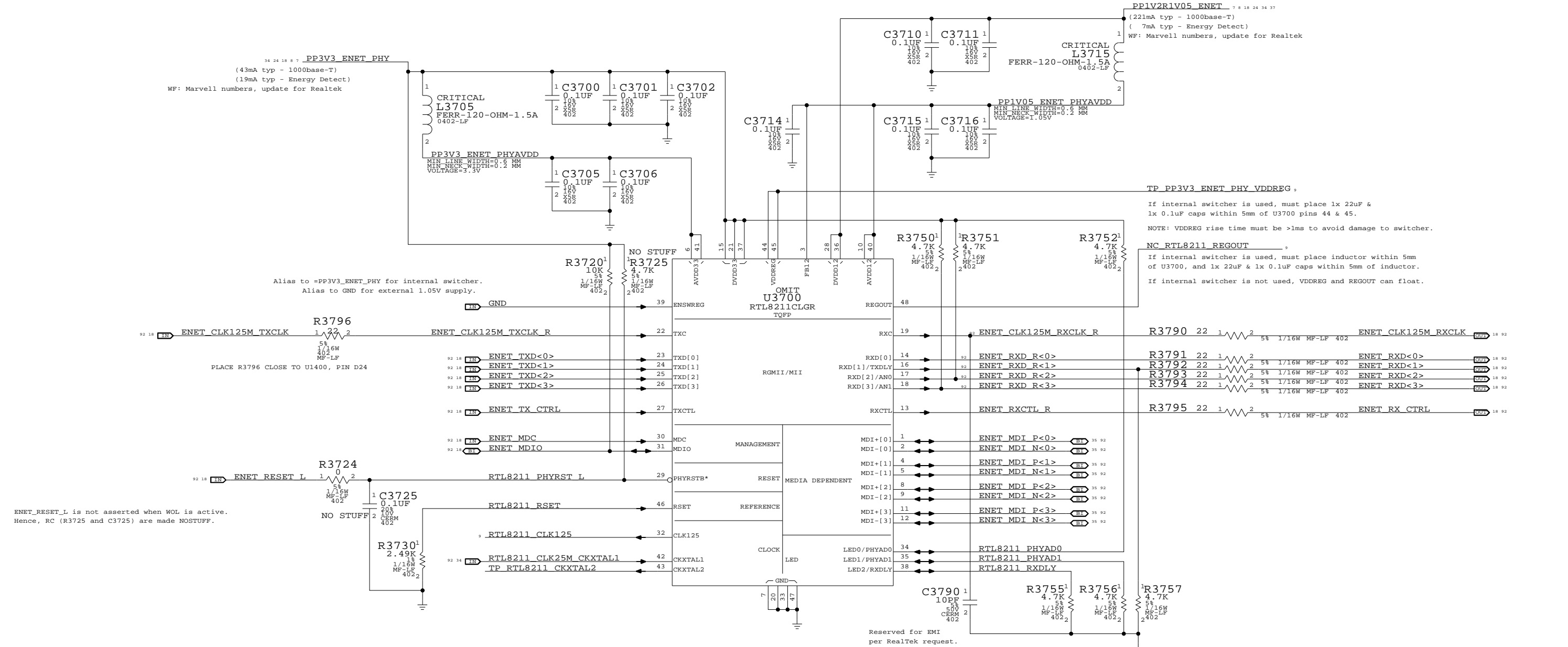
A

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A



Configuration Settings:

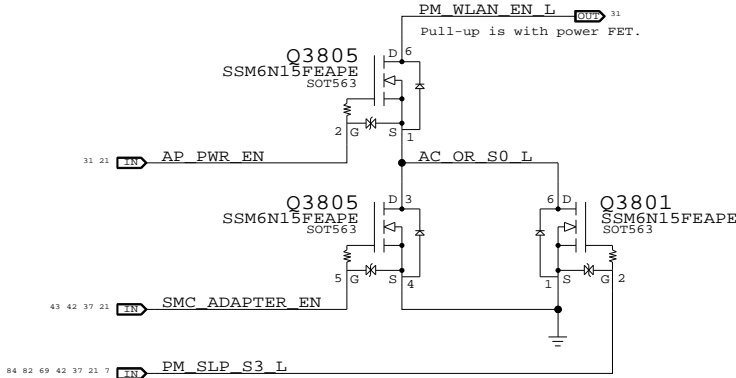
PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

| Ethernet PHY (RTL8211CL) | | |
|--|--|----------------------|
| SYNC_MASTER=SUMA_M98_MLB | | SYNC_DATE=07/01/2008 |
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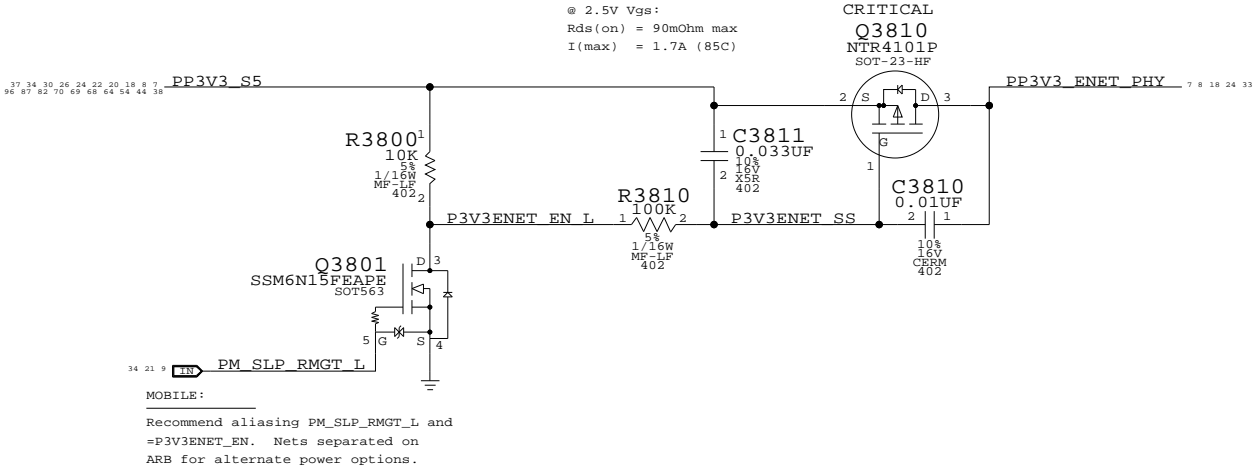
| | | | |
|------------|---------------|----------------------------|---------------|
| APPLE INC. | SIZE D | DRAWING NUMBER 051-7892 | REV. A.0.0 |
| | SCALE NONE | SHT 33 | OF 97 |

WLAN Enable Generation

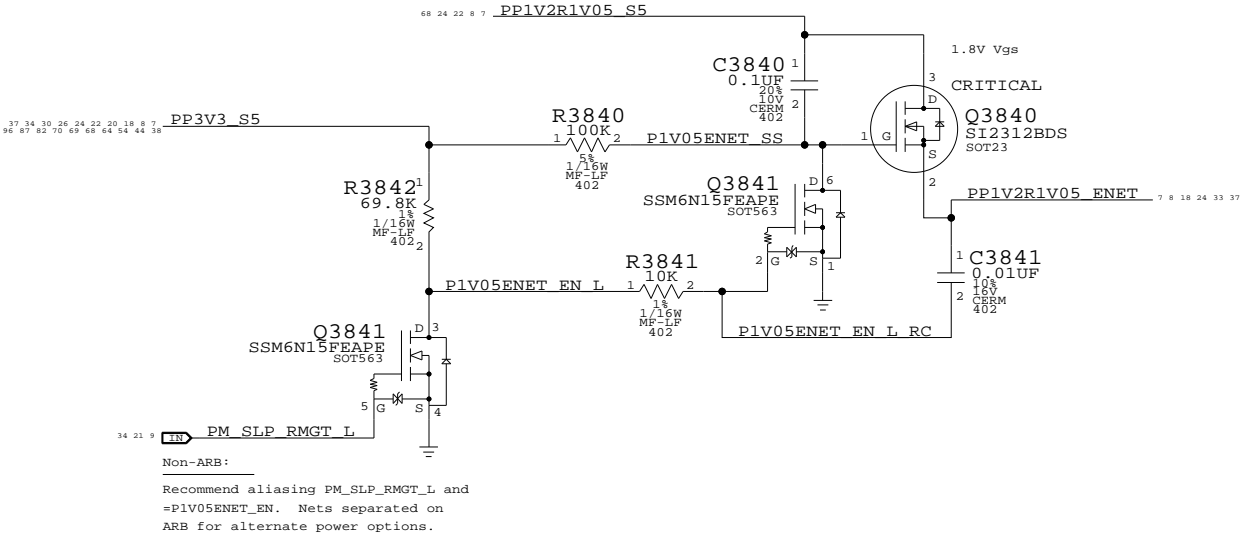
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



3.3V ENET FET

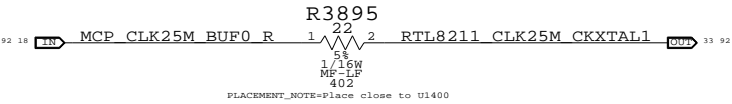


1.05V ENET FET



RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

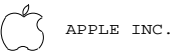


Ethernet & AirPort Support

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

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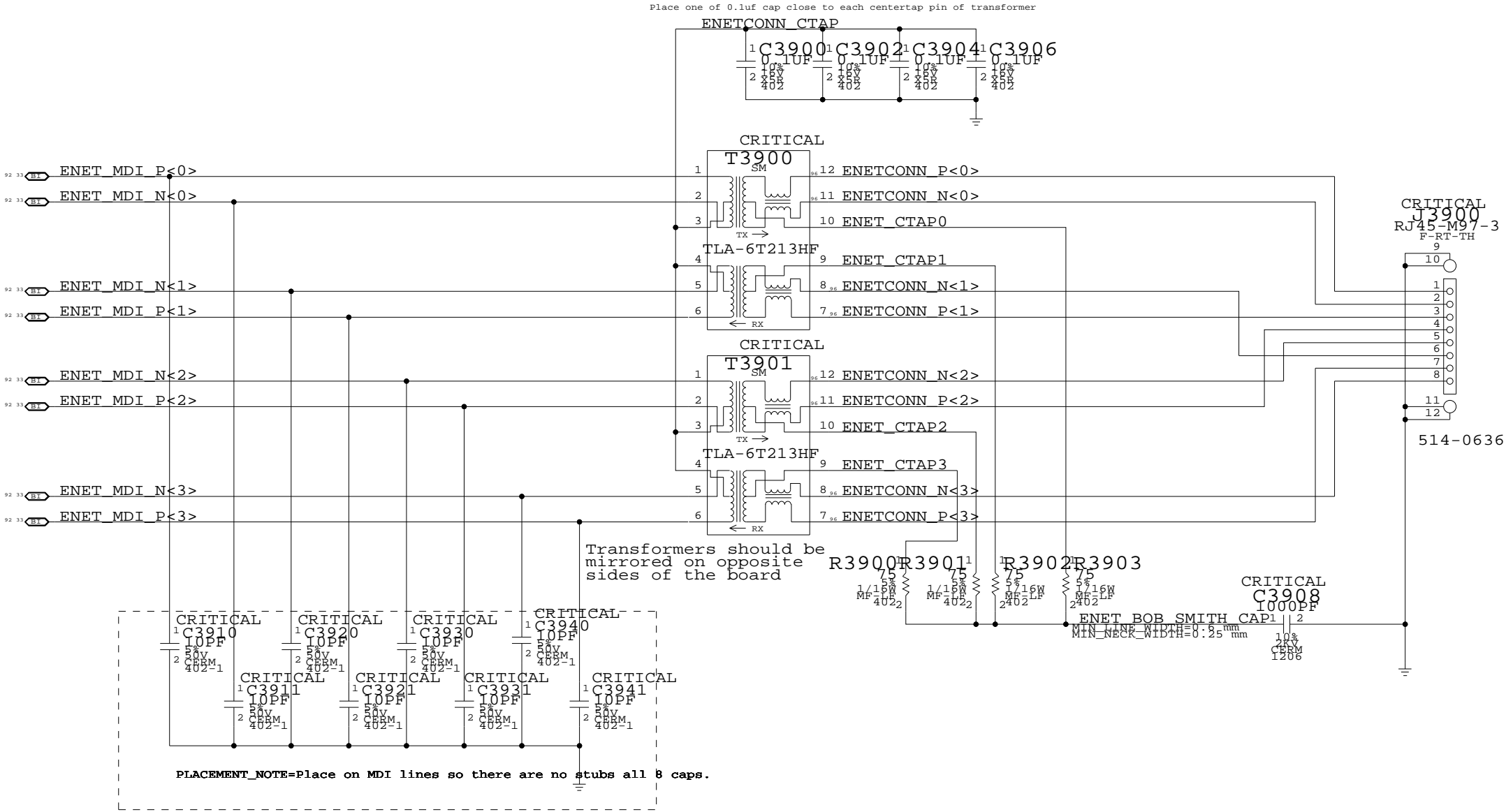
| SIZE | DRAWING NUMBER | REV. |
|-------|----------------|-------|
| D | 051-7892 | A.0.0 |
| SCALE | SHT | OF |
| NONE | 34 | 97 |

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Ethernet Connector

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=12/16/2008

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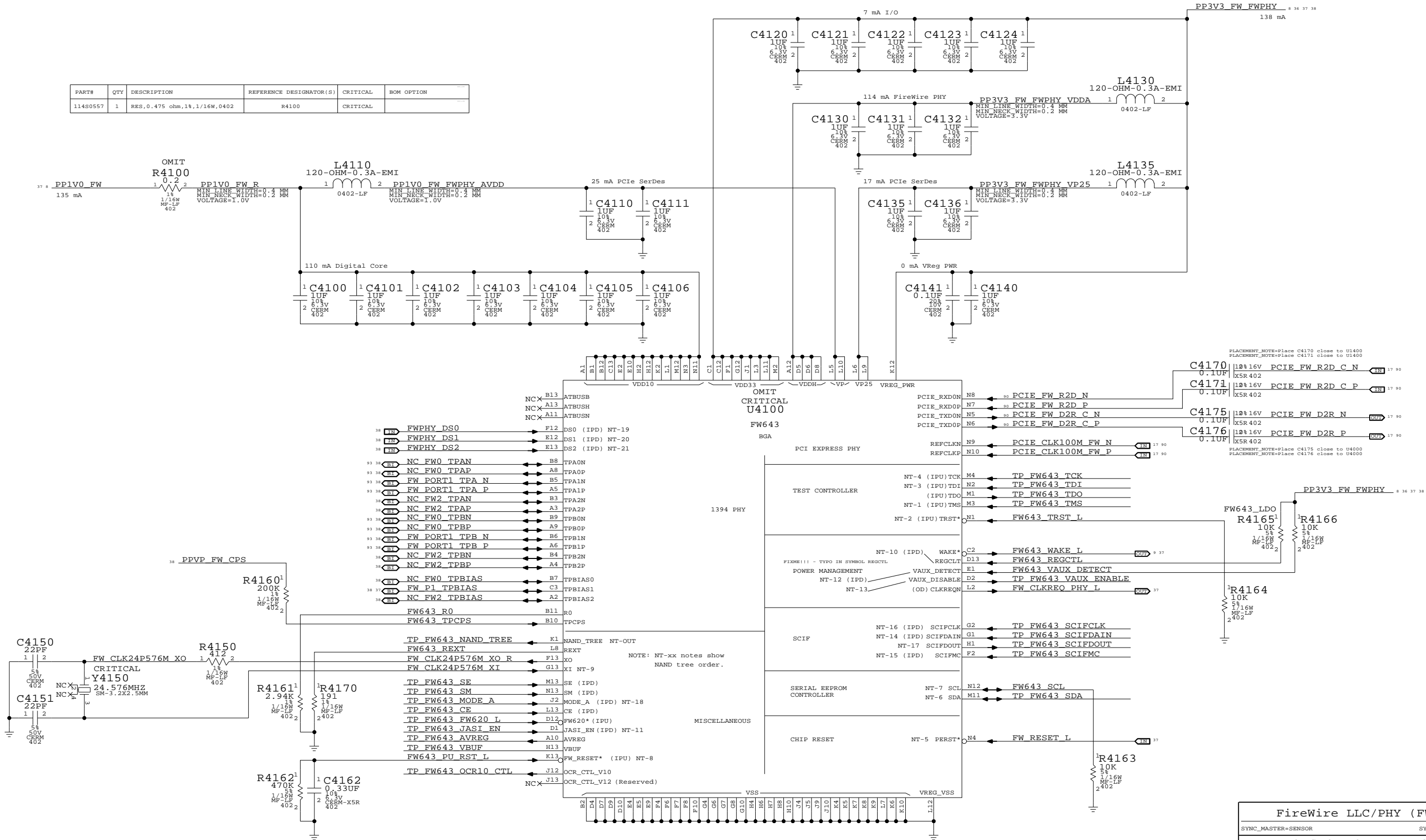
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| NONE | 35 | 97 |

| PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|-----------------------------|-------------------------|----------|------------|
| 11480557 | 1 | RES,0.475 ohm,1%,1/16W,0402 | R4100 | CRITICAL | |



| FireWire LLC/PHY (FW643) | | |
|--|--|----------------------|
| SYNC_MASTER=SENSOR | | SYNC_DATE=08/14/2008 |
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| | | | |
|------------|------|----------------|--------|
| APPLE INC. | SIZE | DRAWING NUMBER | REV. |
| | D | 051-7892 | 4.12.0 |
| SCALE | | SHT | OF |
| NONE | | 36 | 97 |

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVFW_FWSUMODE (power passthru summation mode)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:

3.3V FW FET

@ 2.5V Vgs:

Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

CRITICAL
Q4291
NTR4101P
SOT-23-HF

1.05V FW FET

CRITICAL
Q4295
SI2312BDS
SOT23

FireWire Port Power Switch

Late-VG Event Detection

FireWire Port Power

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| SIZE | DRAWING NUMBER | REV. |
|-------|----------------|-------|
| D | 051-7892 | A.0.0 |
| SCALE | SHT | OF |
| NONE | 37 | 97 |

Page Notes

Power aliases required by this page:

```
- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG
```

```
- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R
```

D Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

```

graph TD
    PP3V3_FW_FWPHY[PP3V3_FW_FWPHY] --- Node1(( ))
    Node1 --- R4382[R4382 10K 1% MF 402]
    Node1 --- R4380[R4380 10K 1% MF 402]
    Node1 --- FWPHY_DS0[FWPHY_DS0]
    FWPHY_DS0 --- MAKE_BASE_TRUE[MAKE_BASE=TRUE]
    Node1 --- FWPHY_DS2[FWPHY_DS2]
    FWPHY_DS2 --- FWPHY_DS2_STRAP[FWPHY_DS2]
  
```

38 37 36 8 PP3V3_FW_FWPHY

R4382¹
10K
1%
MF 402²

R4380¹
10K
1%
MF 402²

38 36 FWPHY_DS0 — FWPHY_DS0 36 38
MAKE_BASE=TRUE

38 36 FWPHY_DS2 — FWPHY_DS2 36 38

```

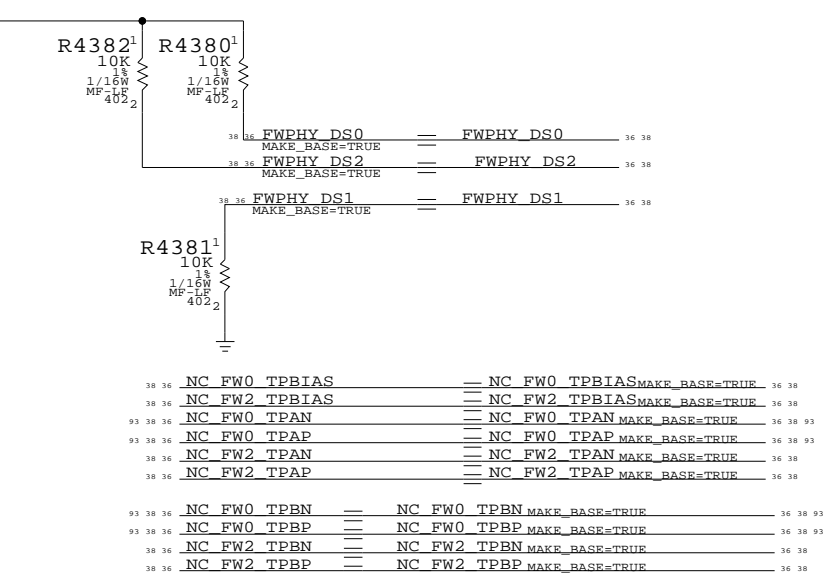
Configures PHY for:

```

- ```

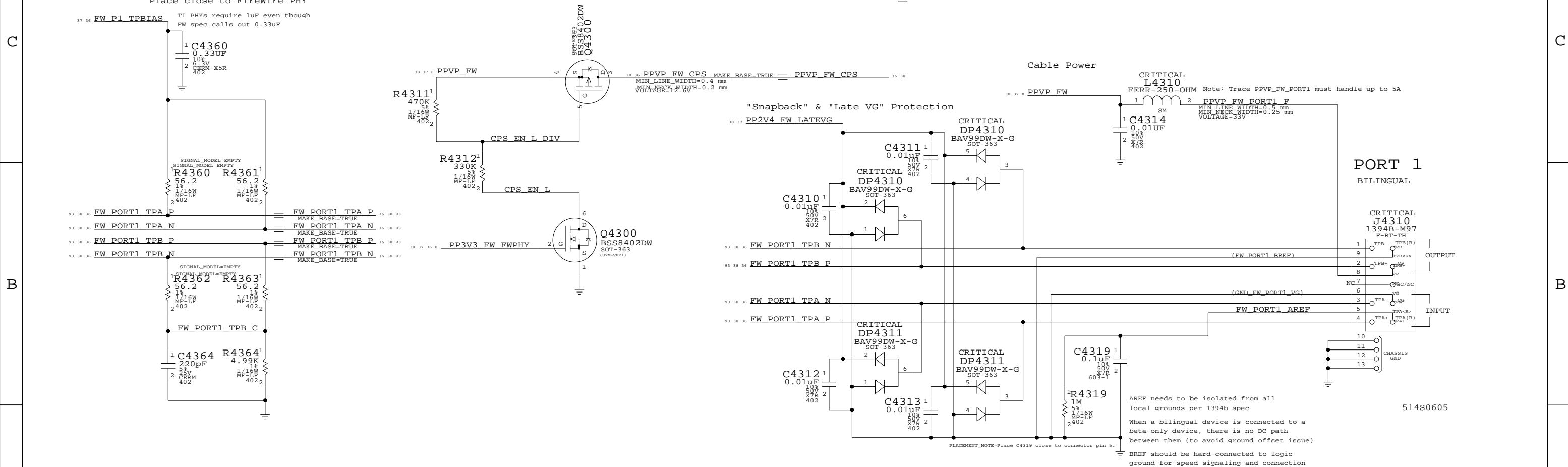
- 1-port Portable Power Class (0)
- Port "1" Bilingual (1394B)

```

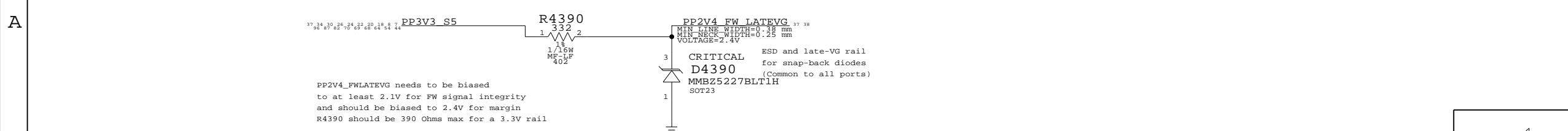


## Termination

Place close to FireWire PHY



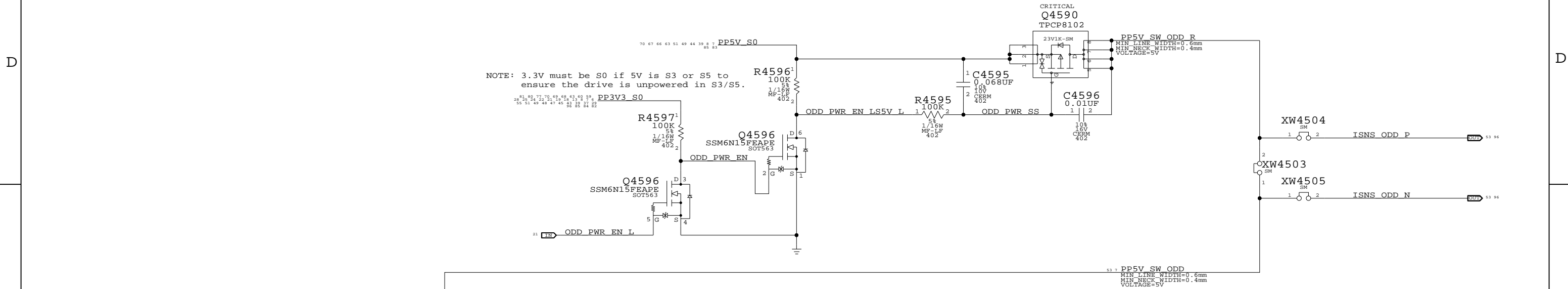
Late-VG Protection Power



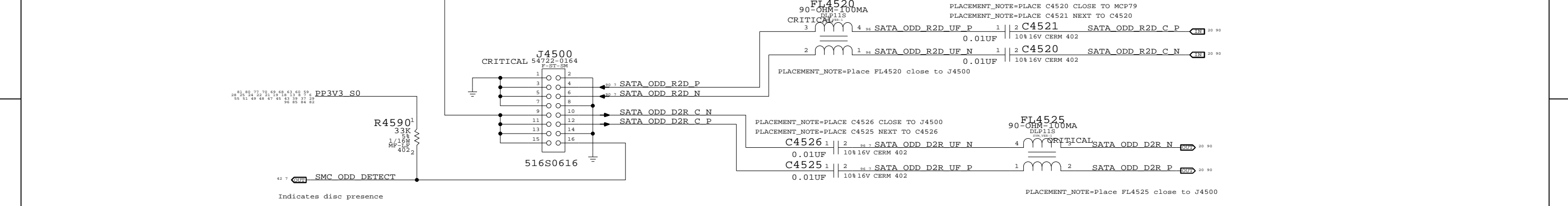
|                                                                                                                                  |      |                     |       |
|----------------------------------------------------------------------------------------------------------------------------------|------|---------------------|-------|
| FireWire Ports                                                                                                                   |      |                     |       |
| SYN_MASTER=SENSOR                                                                                                                |      | SYN_DATE=08/14/2008 |       |
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| D                                                                                                                                | SIZE | DRAWING NUMBER      | REV.  |
|                                                                                                                                  |      | 051-7892            | A.0.0 |
| SCALE                                                                                                                            | SHT  | OF                  |       |
| NONE                                                                                                                             | 38   | 97                  |       |



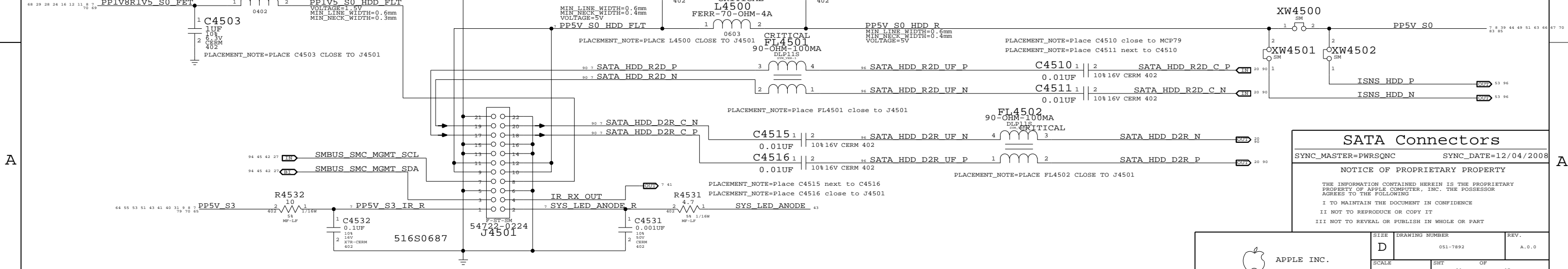
ODD Power Control



SATA ODD Port



SATA HDD Port

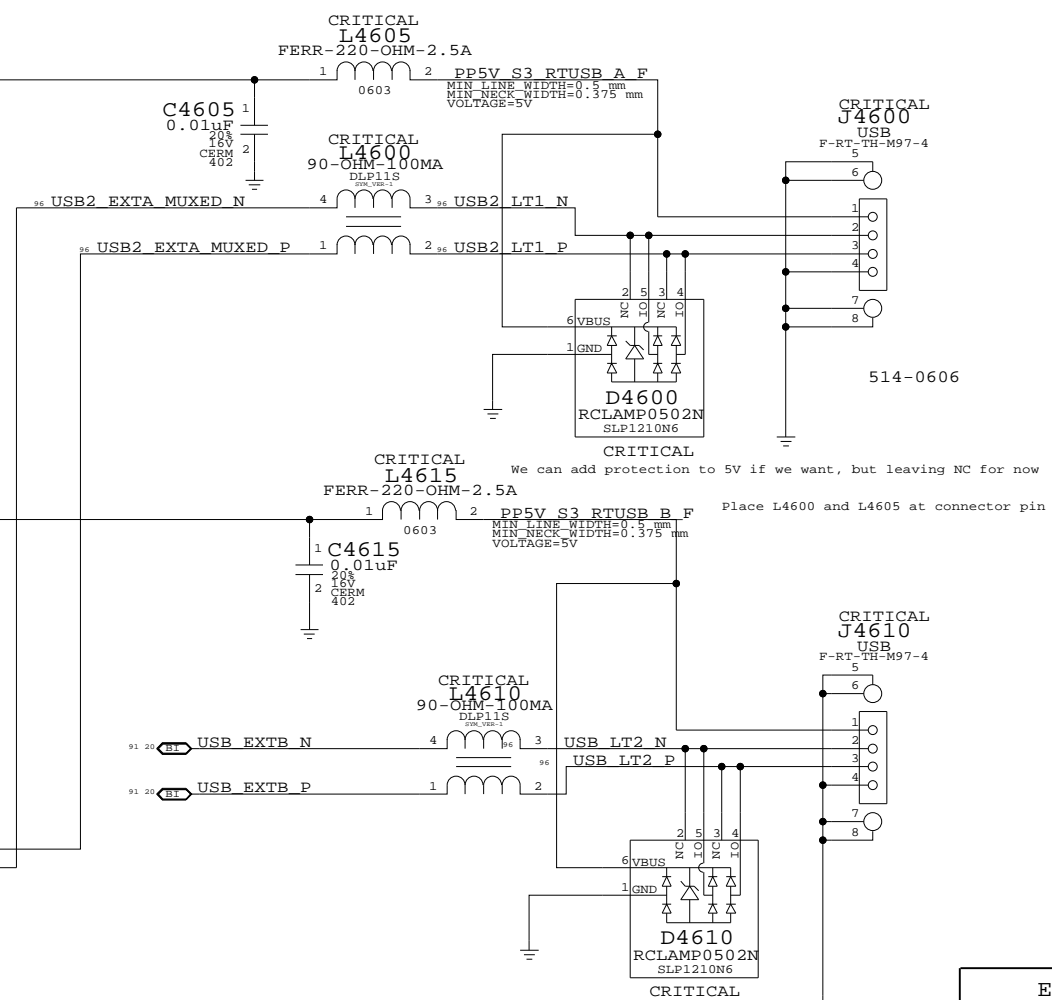


| SATA Connectors                                                                                                            |  |                      |
|----------------------------------------------------------------------------------------------------------------------------|--|----------------------|
| SYNC_MASTER=PWRSONC                                                                                                        |  | SYNC_DATE=12/04/2008 |
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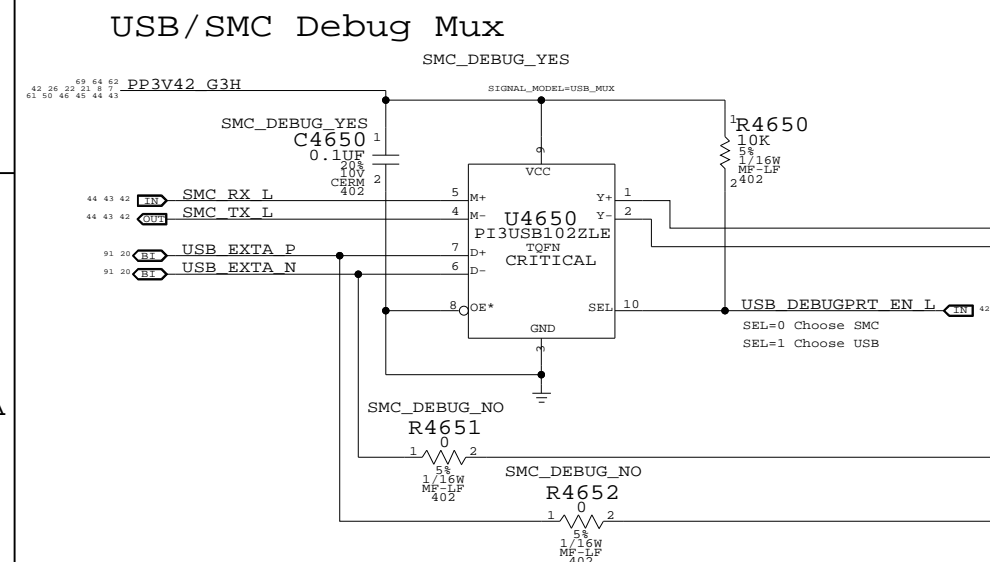
|            |      |                |       |
|------------|------|----------------|-------|
| APPLE INC. | SIZE | DRAWING NUMBER | REV.  |
|            | D    | 051-7892       | A.0.0 |
| SCALE      |      | SHT            | OF    |
| NONE       |      | 39             | 97    |



Left USB Port A



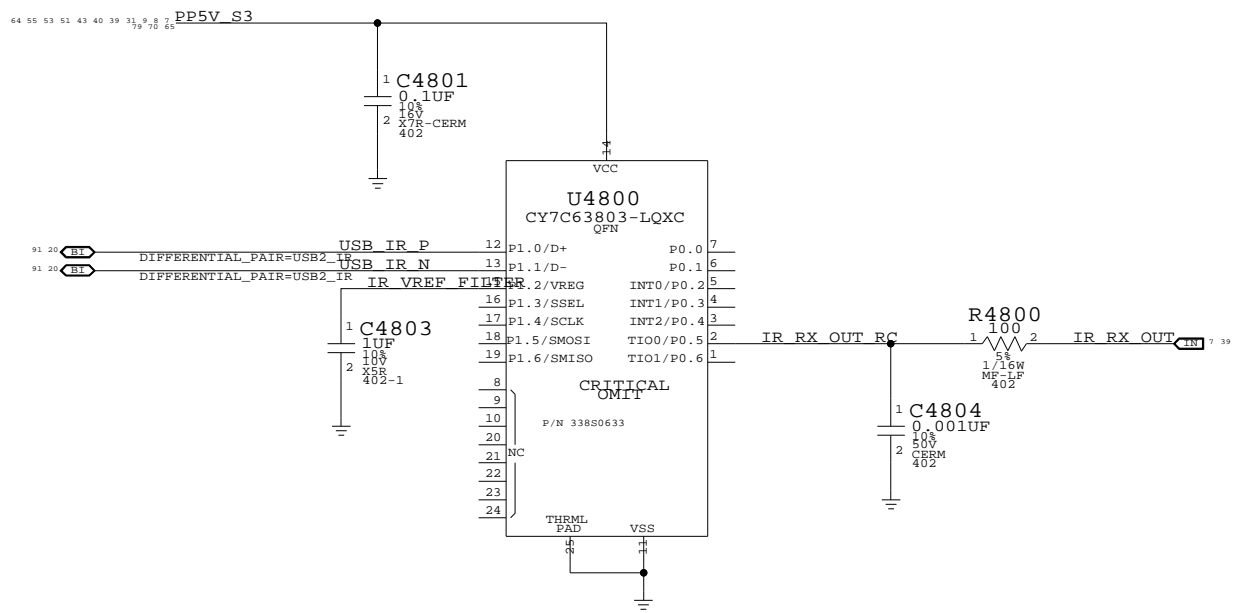
Left USB Port B



|                                                                                                                                  |                      |
|----------------------------------------------------------------------------------------------------------------------------------|----------------------|
| External USB Connectors                                                                                                          |                      |
| SYNC_MASTER=M98_MLB                                                                                                              | SYNC_DATE=11/14/2008 |
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IR SUPPORT



Front Flex Support

SYNC\_MASTER=PWRSONC SYNC\_DATE=12/04/2008

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SIZE  
D

DRAWING NUMBER  
051-7892

REV.

A.0.0

SCALE  
NONE

SHT  
41

OF  
97



NOTE: Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

D

C

B

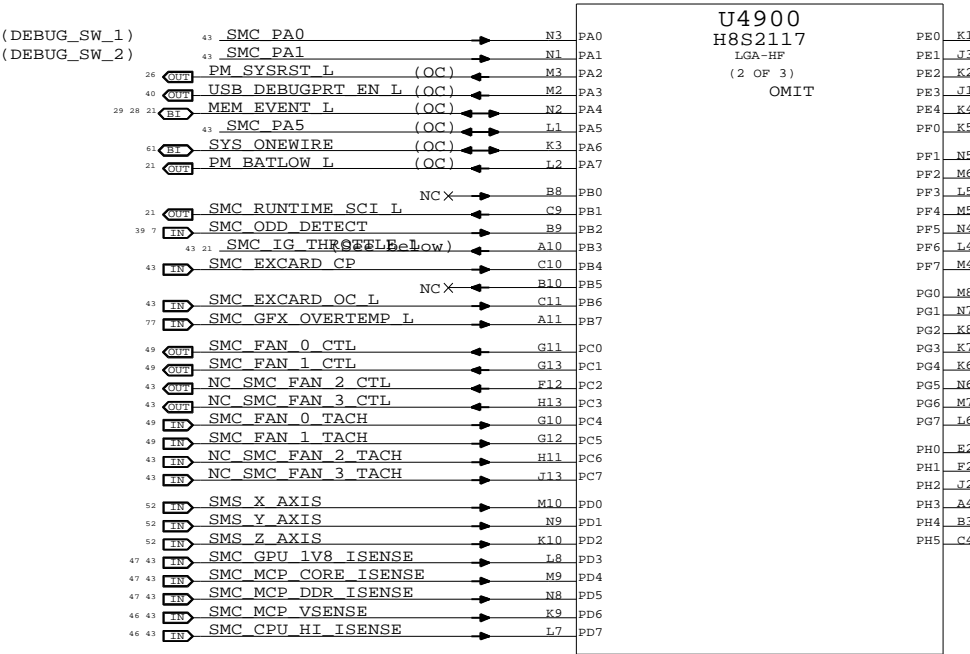
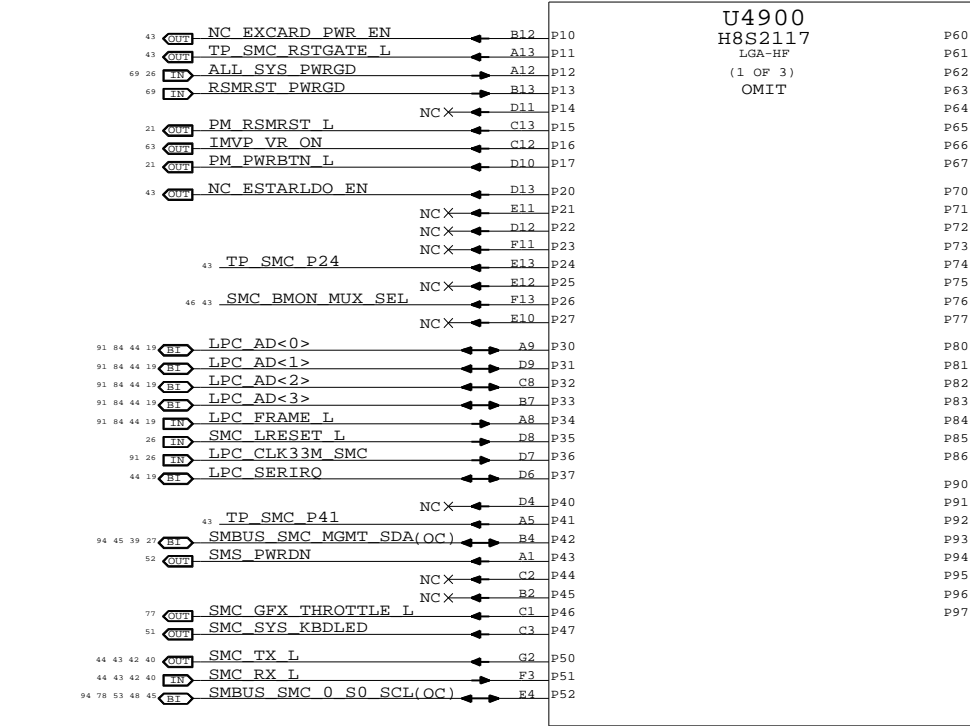
A

D

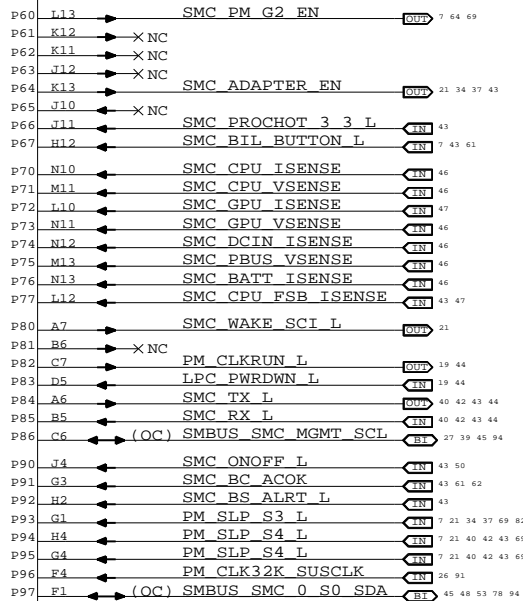
C

B

A

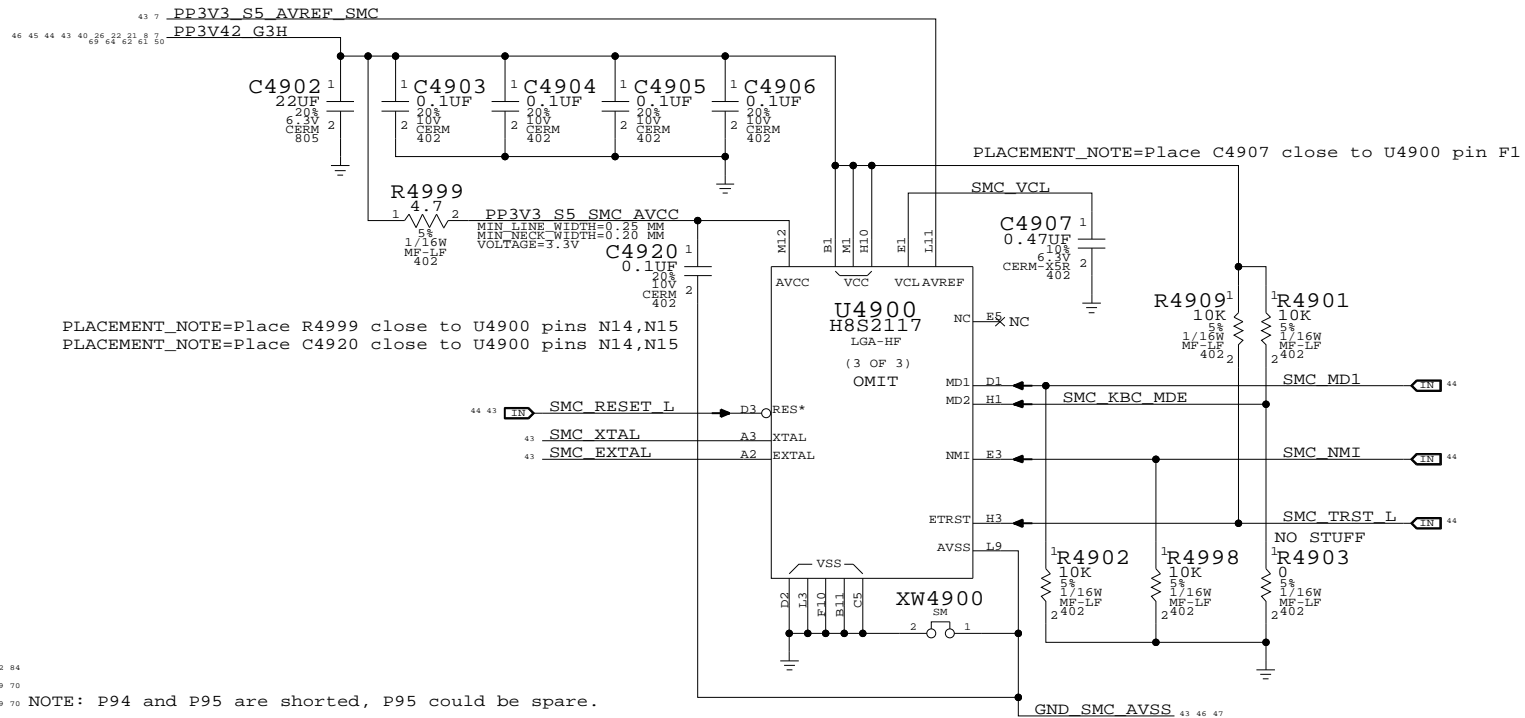


SMC\_PB3:  
SMC\_IG\_THROTTLE\_L for MG systems.  
Otherwise, TP/NC okay (was ISENSE\_CAL\_EN)



PLACEMENT\_NOTE=Place R4999 close to U4900 pins N14,N15  
PLACEMENT\_NOTE=Place C4920 close to U4900 pins N14,N15

NOTE: P94 and P95 are shorted, P95 could be spare.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.  
If SMS interrupt is not used, pull up to SMC rail.

SMC

SYNC\_MASTER=T18\_MLB SYNC\_DATE=12/12/2008

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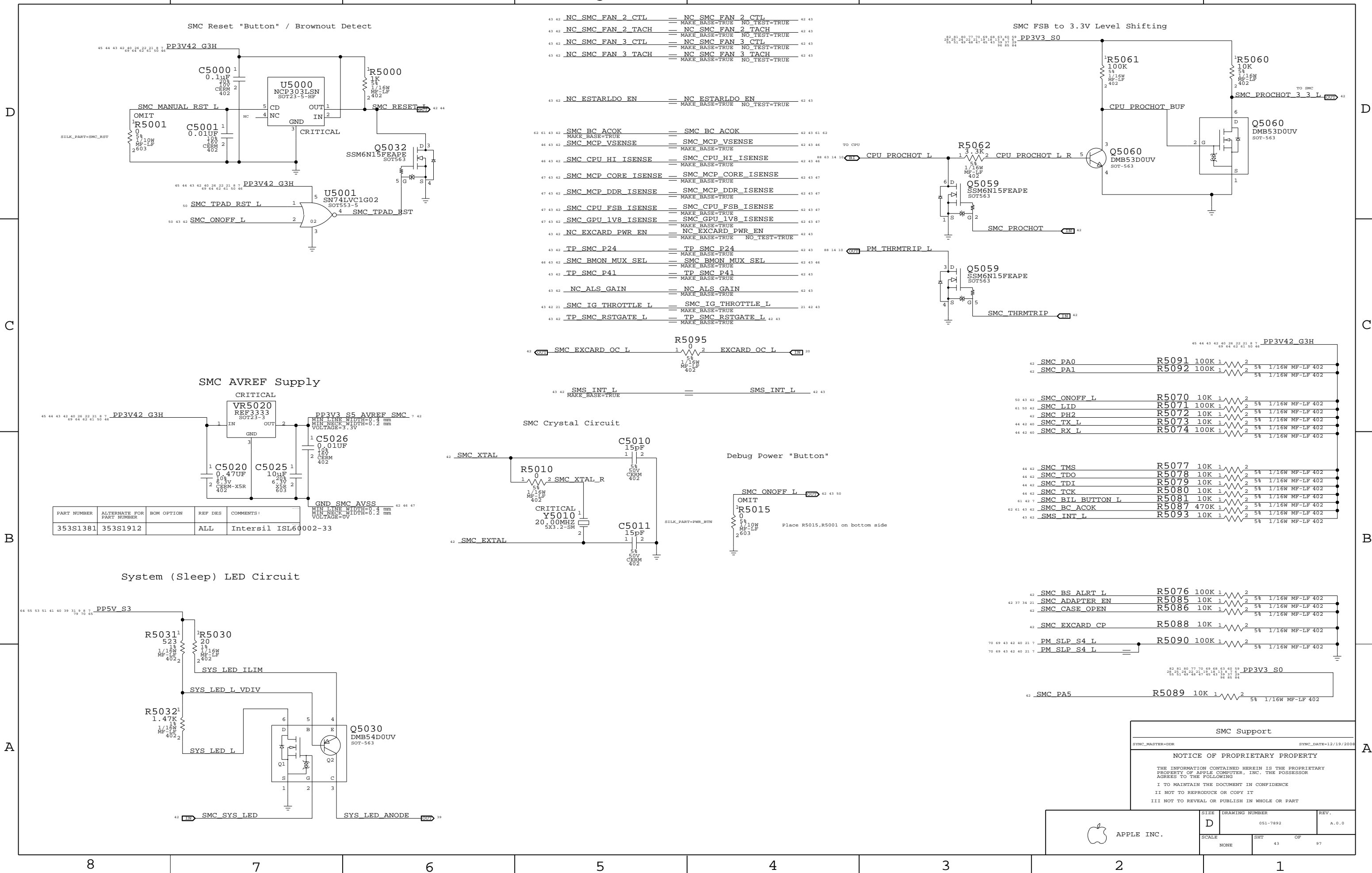
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

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SIZE D DRAWING NUMBER 051-7892 REV. A.0.0

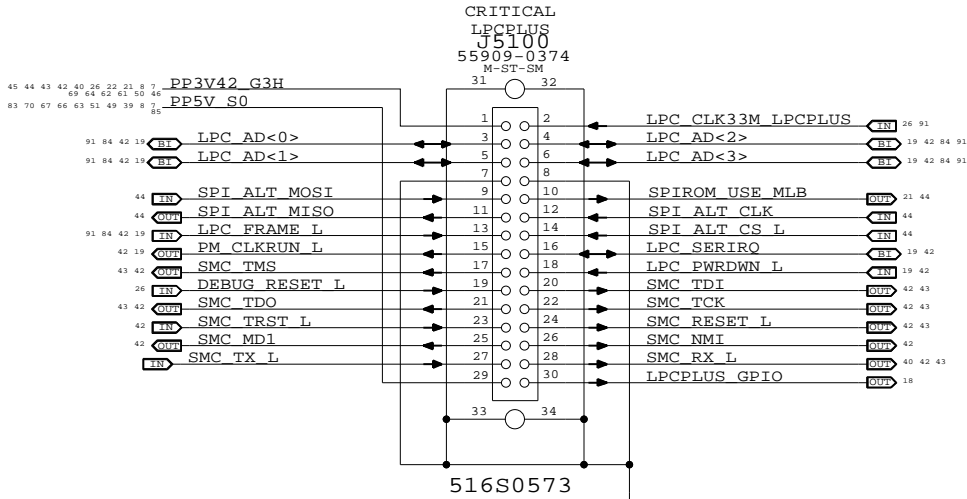
SCALE NONE SHT 42 OF 97



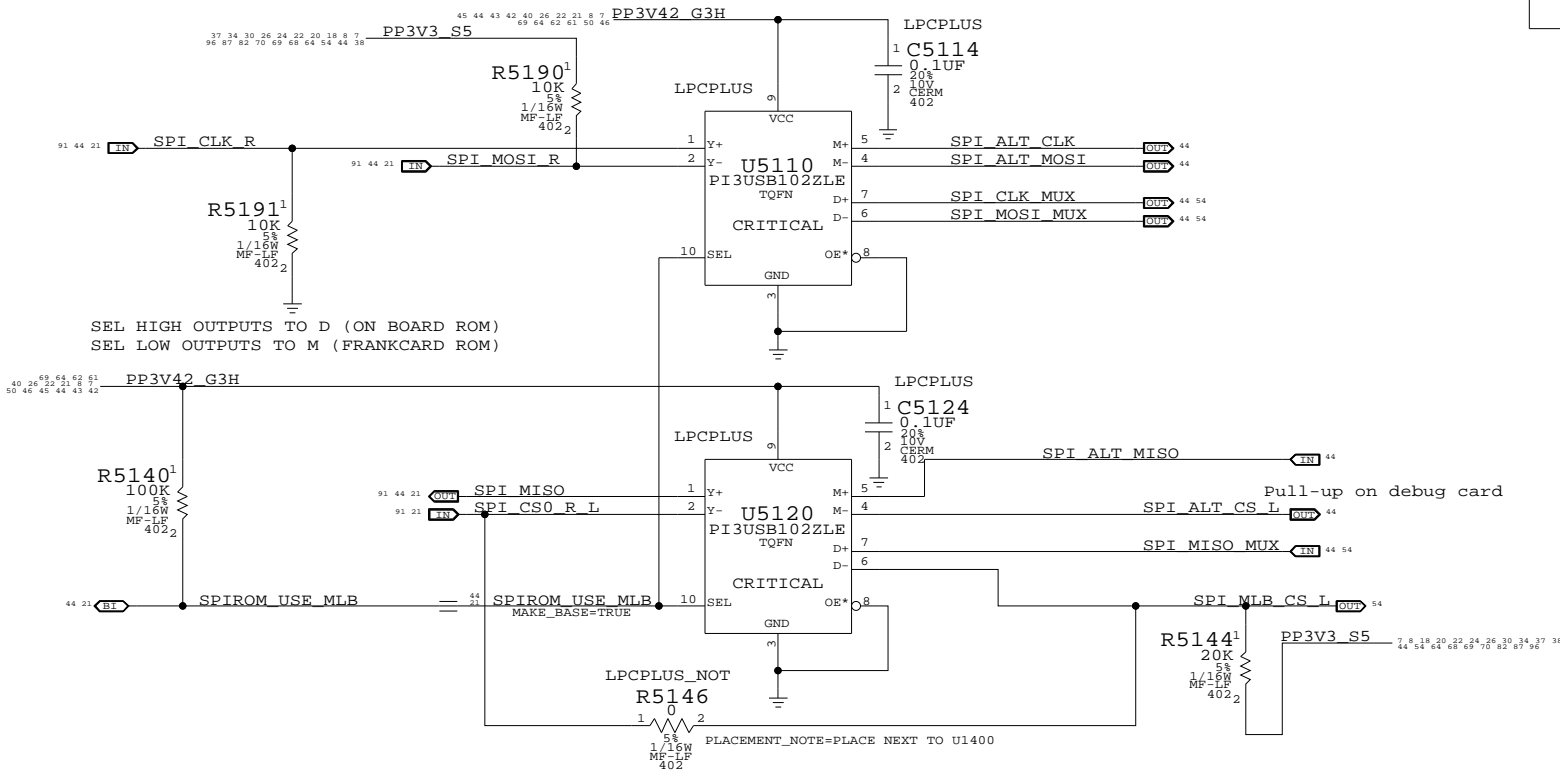




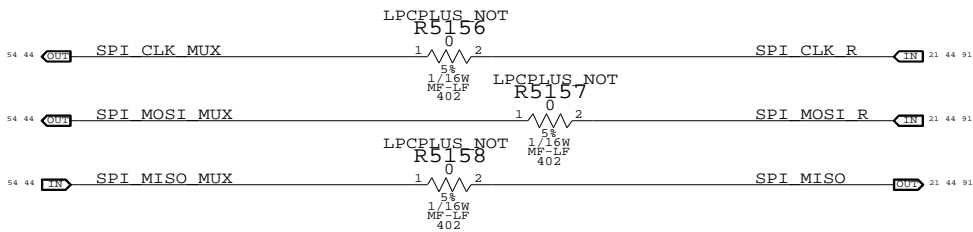
LPC+SPI Connector



Alternate SPI ROM Support



SPI MUX BYPASS



LPC+SPI Debug Connector

SYNC\_MASTER=CHANGZHANG SYNC\_DATE=05/09/2008

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SIZE

D

SCALE

NONE

DRAWING NUMBER

051-7892

SHT

44

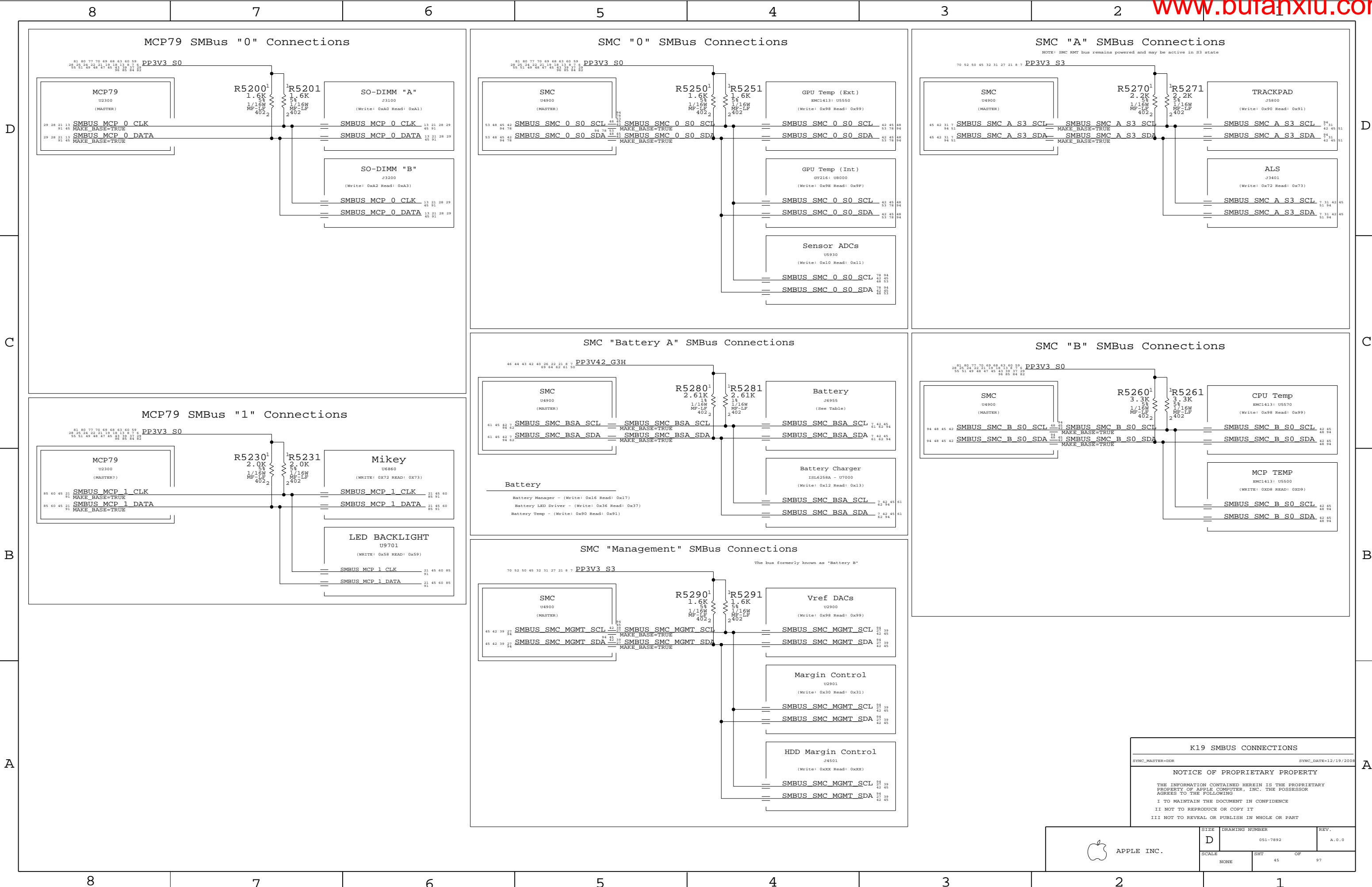
OF

97

REV.

A.0.0





K19 SMBUS CONNECTIONS

SYNC\_MASTER=DOR SYNC\_DATE=12/19/2008

NOTICE OF PROPRIETARY PROPERTY

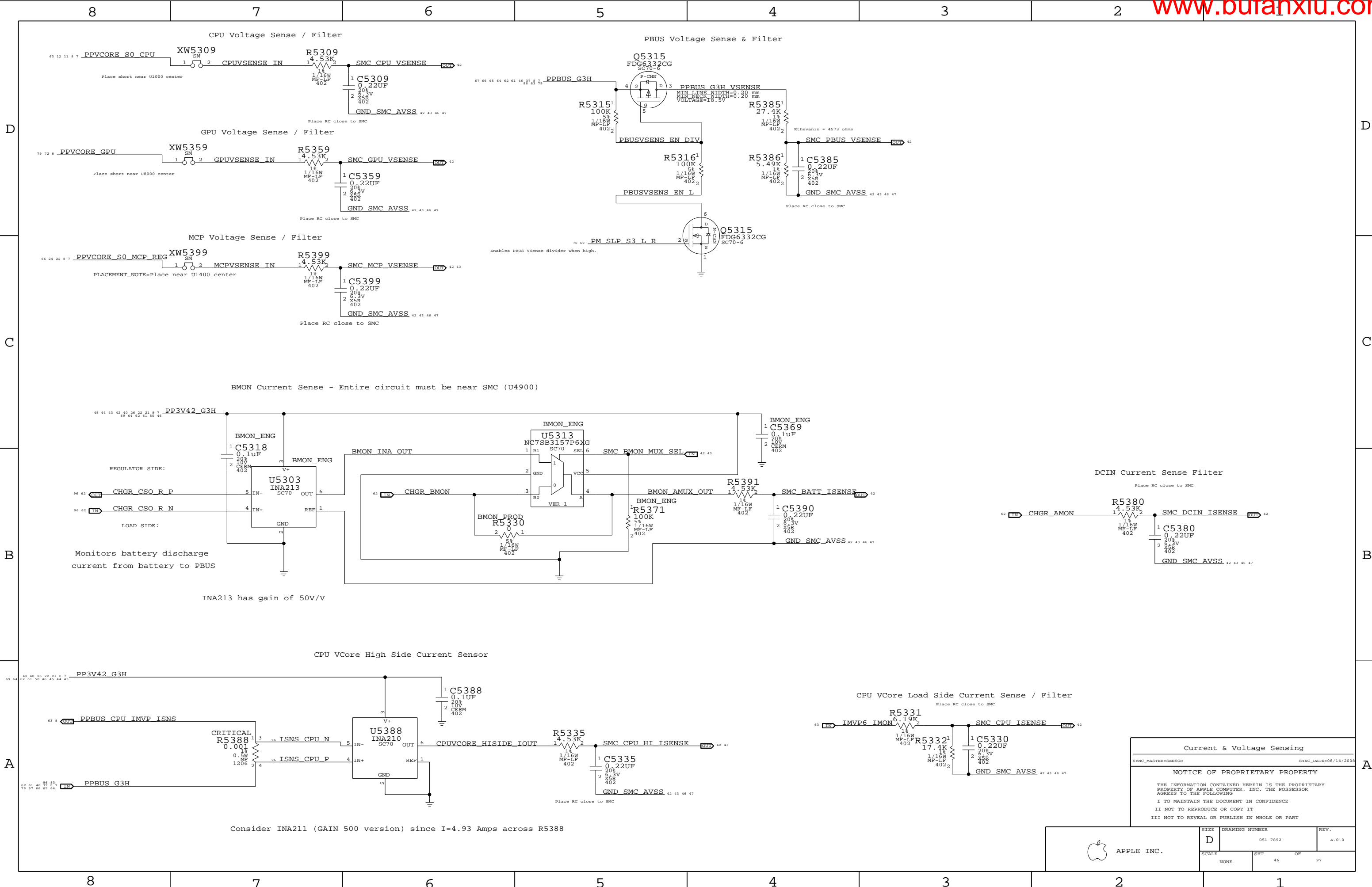
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Current & Voltage Sensing

SYNC\_MASTER=SENSOR SYNC\_DATE=08/14/2008

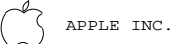
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| NONE  | 46             | 97    |



D

D

C

C

B

B

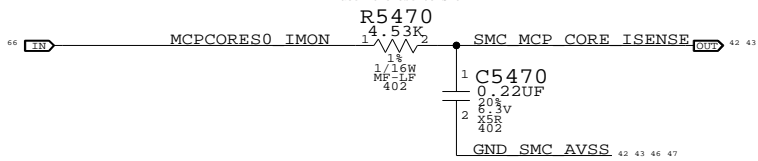
A

A

MCP VCore Current Sense

MCP VCore Current Sense Filter

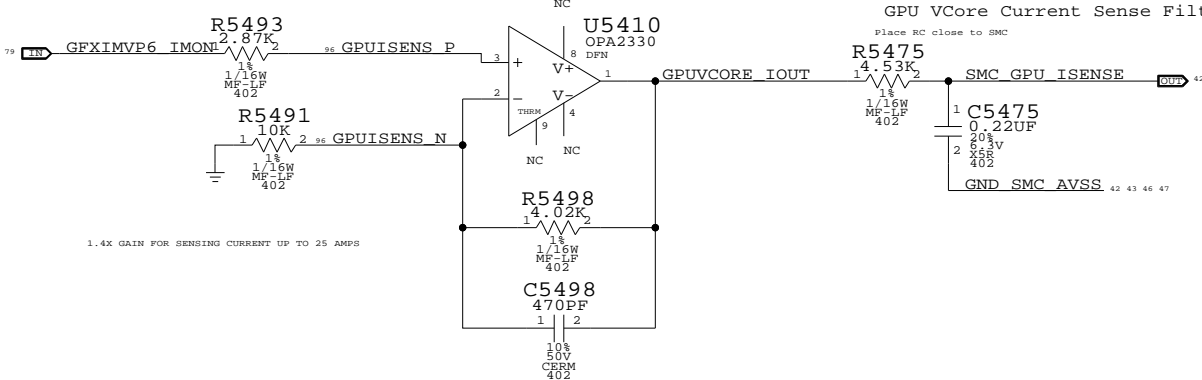
Place RC close to SMC



GPU VCore Current Sense

GPU VCore Current Sense Filter

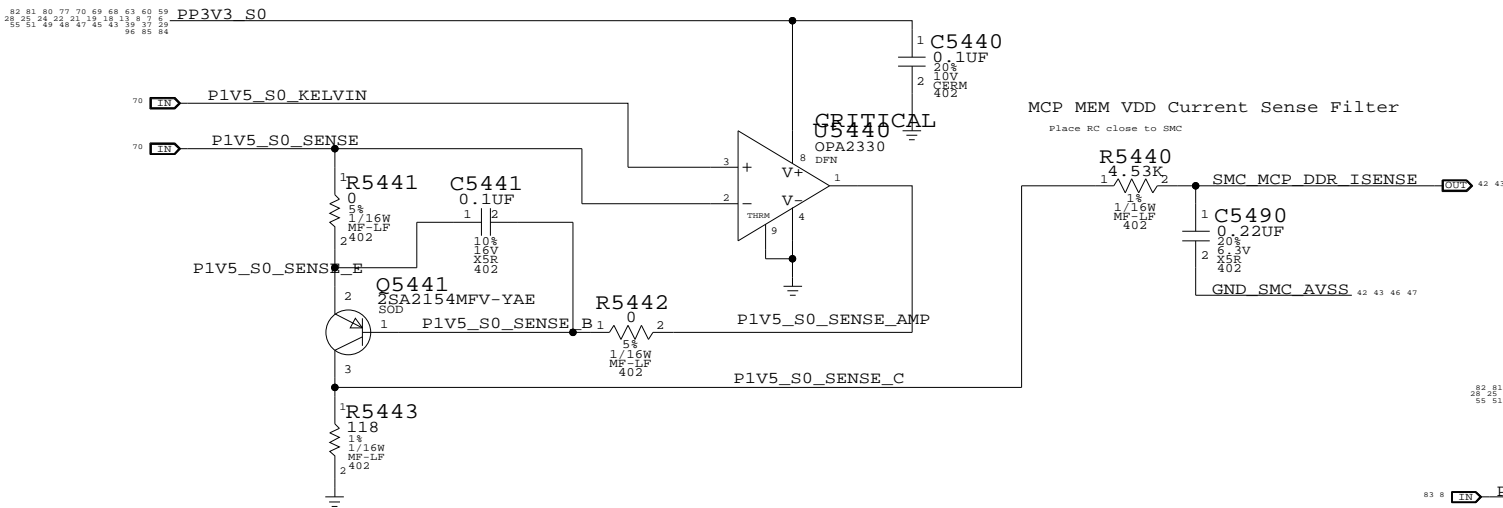
Place RC close to SMC



MCP MEM VDD Current Sense

MCP MEM VDD Current Sense Filter

Place RC close to SMC

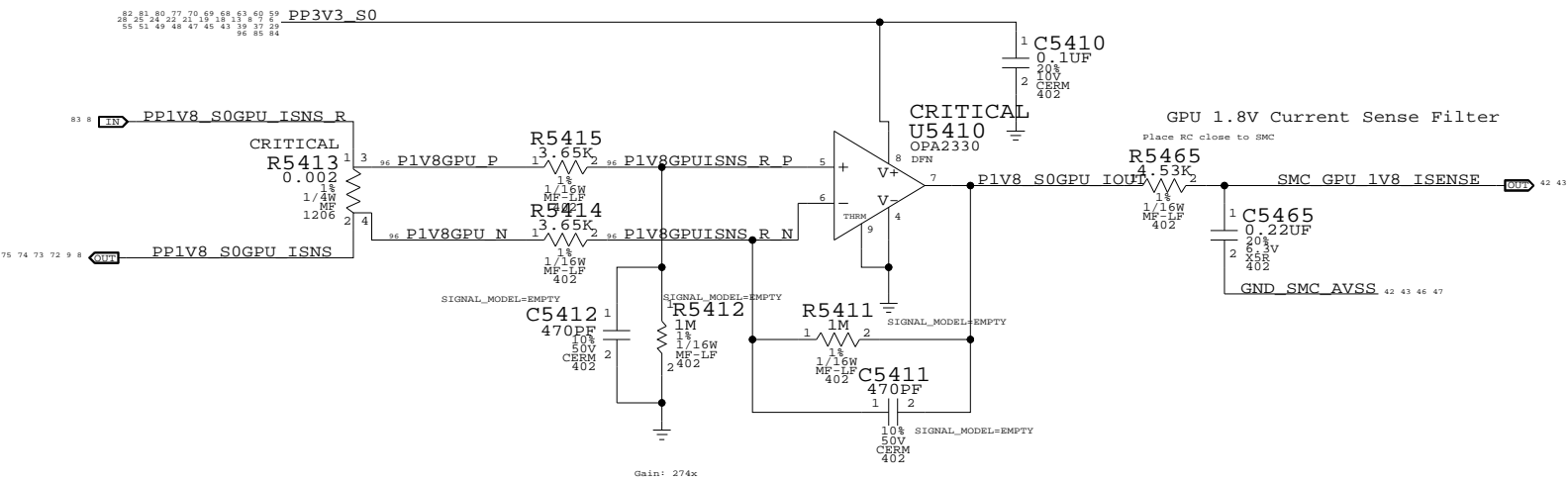


GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

GPU 1.8V Current Sense

GPU 1.8V Current Sense Filter

Place RC close to SMC

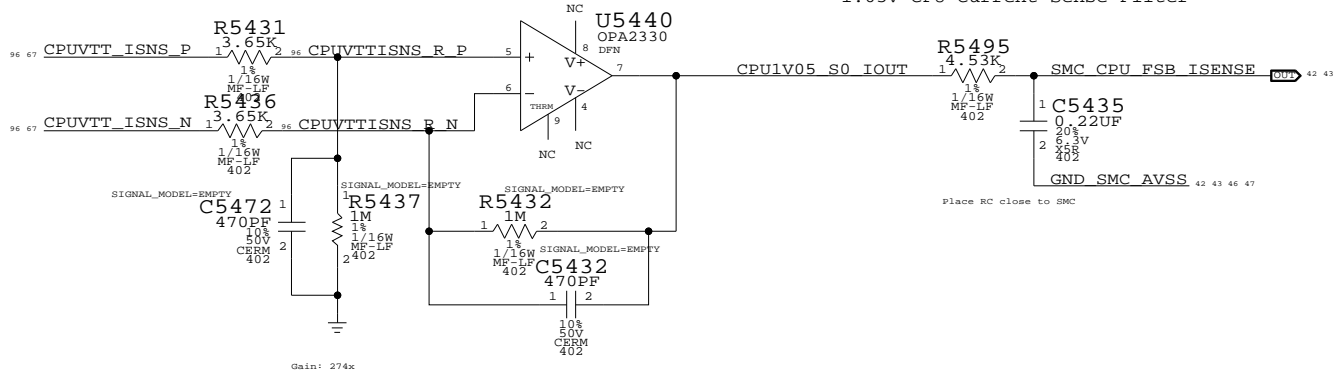


MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

CPU FSB 1.05V Current Sense

1.05V CPU Current Sense Filter

Place RC close to SMC



| Current Sensing                                                                                                            |  |                      |
|----------------------------------------------------------------------------------------------------------------------------|--|----------------------|
| SYNC_MASTER=YUN_K19_MLB                                                                                                    |  | SYNC_DATE=12/10/2008 |
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| SCALE | SHT            | OF    |
| NONE  | 47             | 97    |



## D



## C

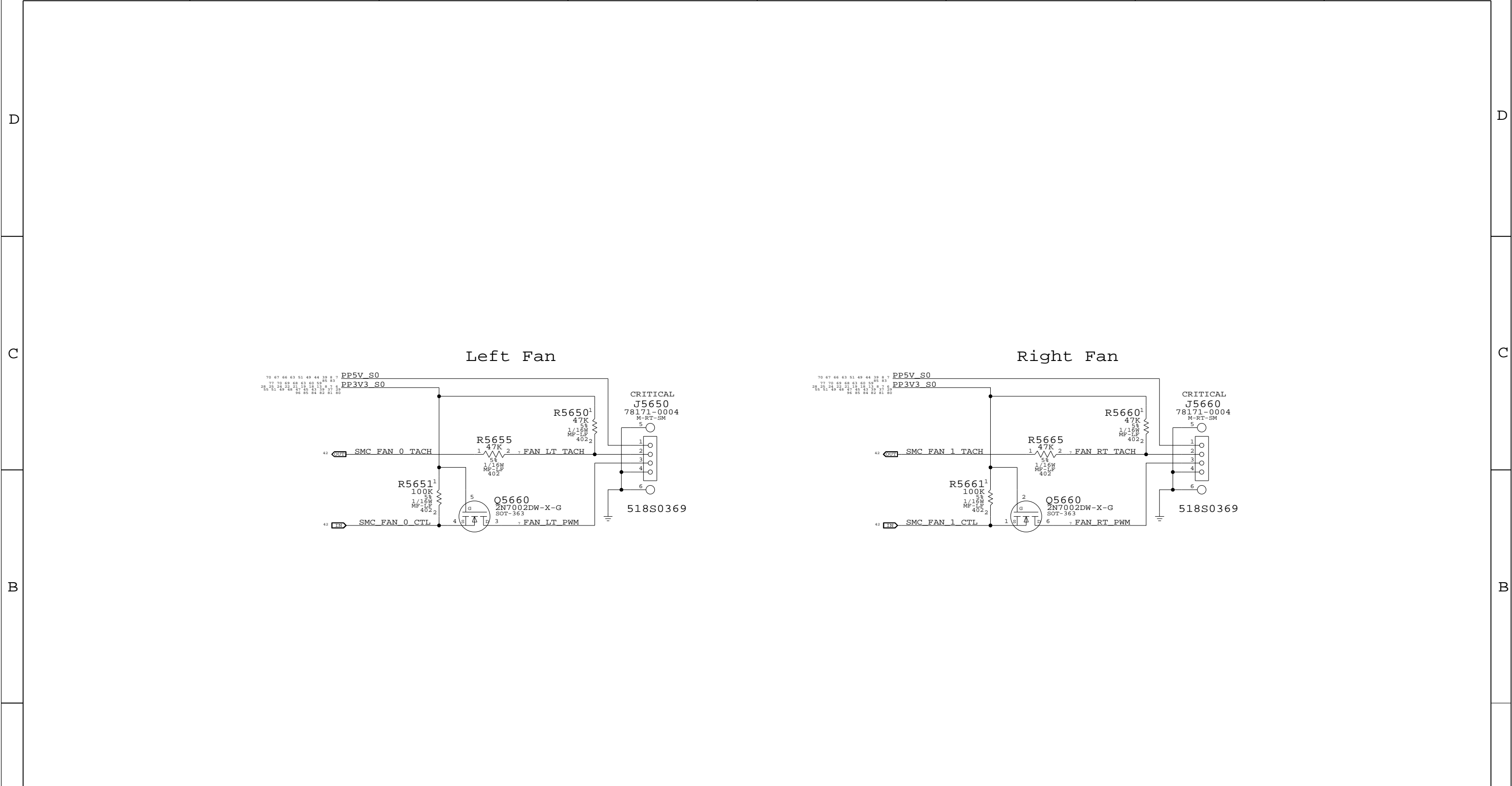
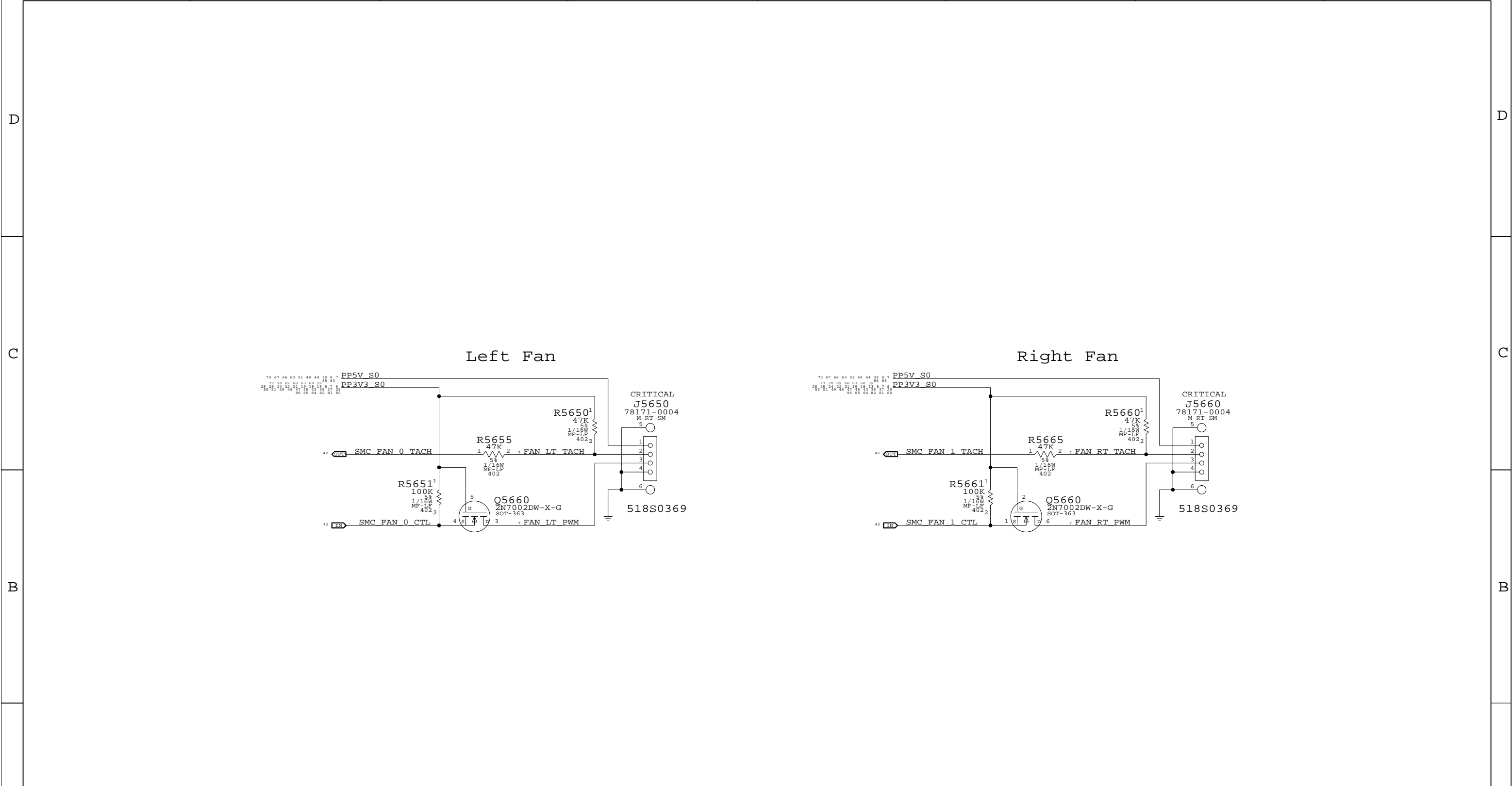


## B

A

|   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 |
|---|---|---|---|---|---|---|





| Fan Connectors      |                      |
|---------------------|----------------------|
| SYNC_MASTER=M87_MLB | SYNC_DATE=10/17/2007 |

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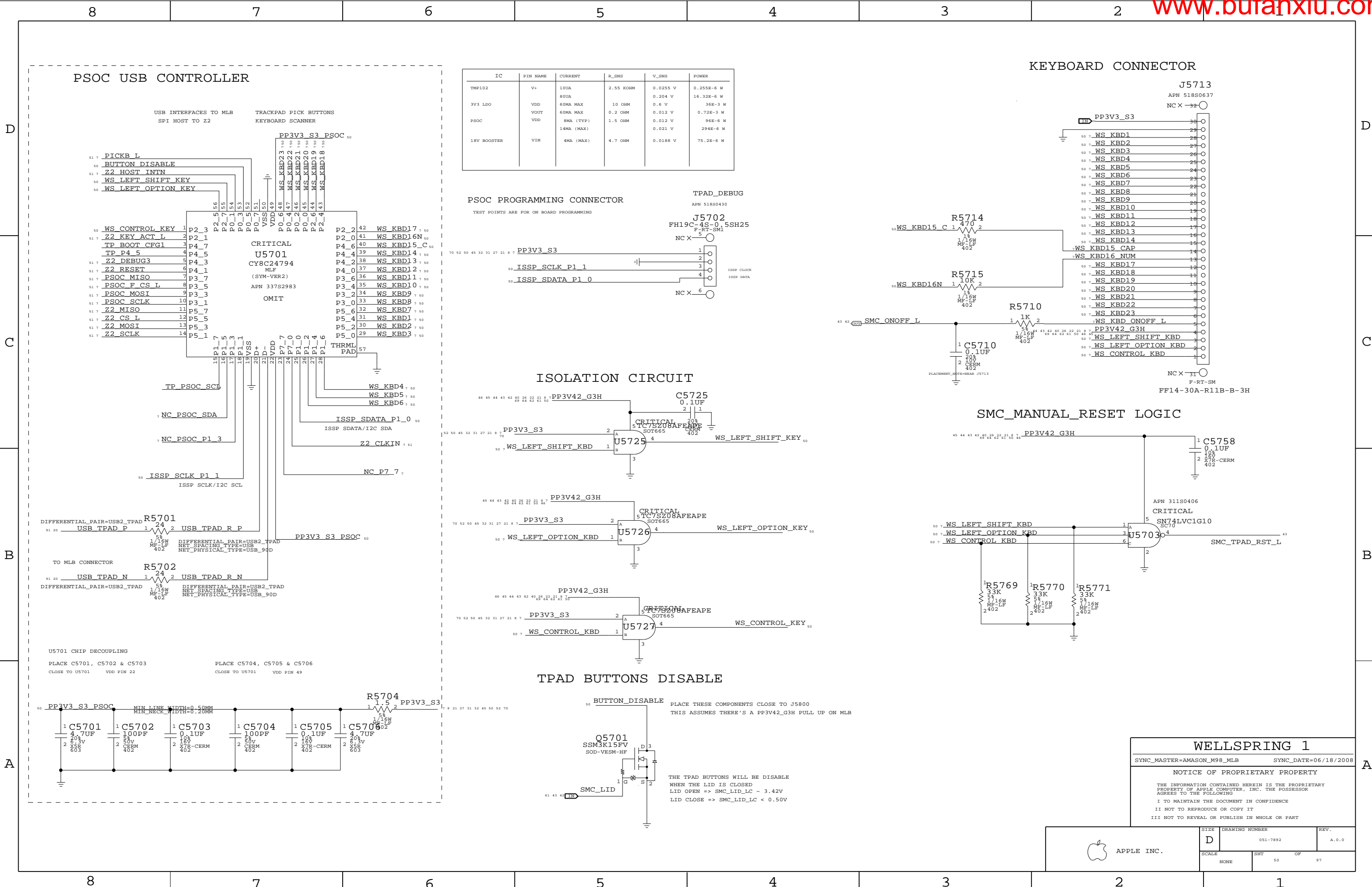
|  |      |                |      |
|--|------|----------------|------|
|  | SIZE | DRAWING NUMBER | REV. |
|--|------|----------------|------|

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|       |     |    |
|-------|-----|----|
| SCALE | SHT | OF |
|       | 40  | 03 |

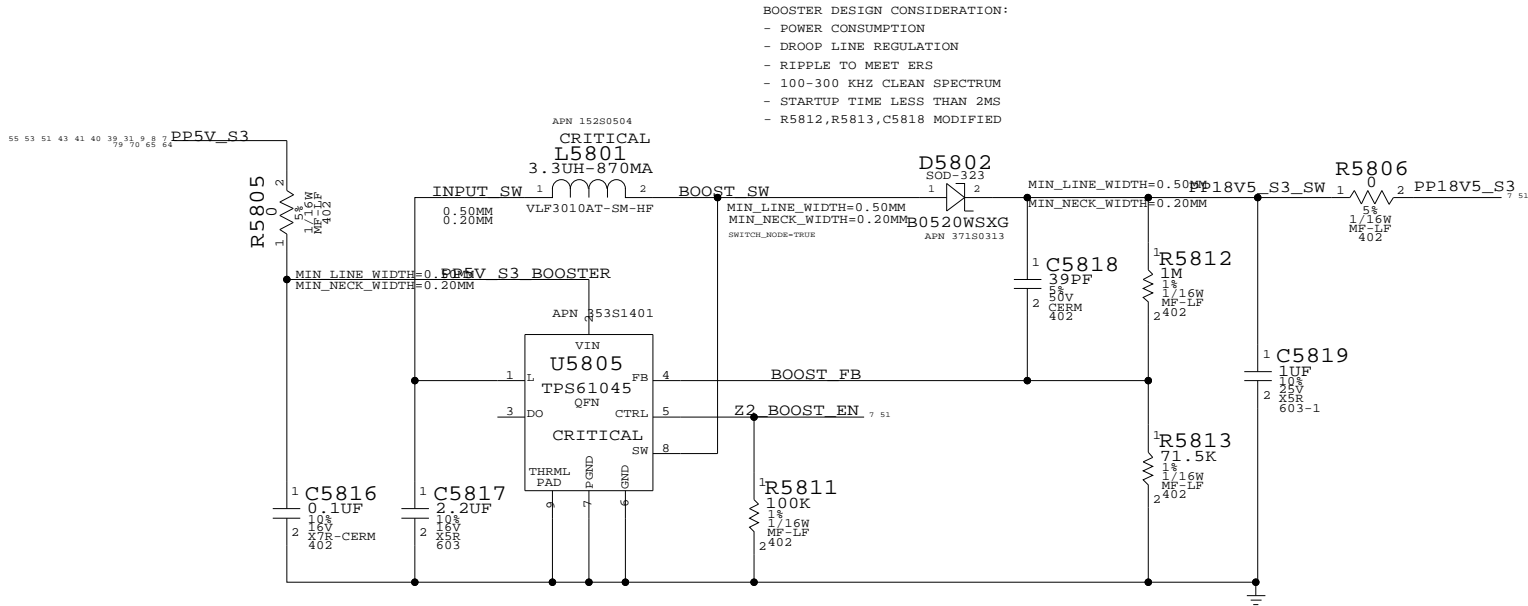
|      |    |    |
|------|----|----|
| NONE | 49 | 57 |
|------|----|----|



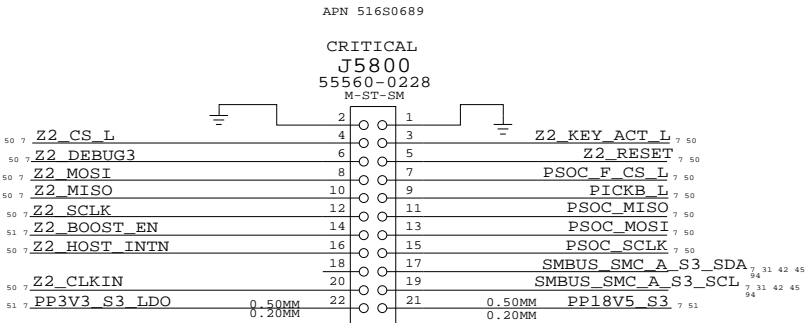




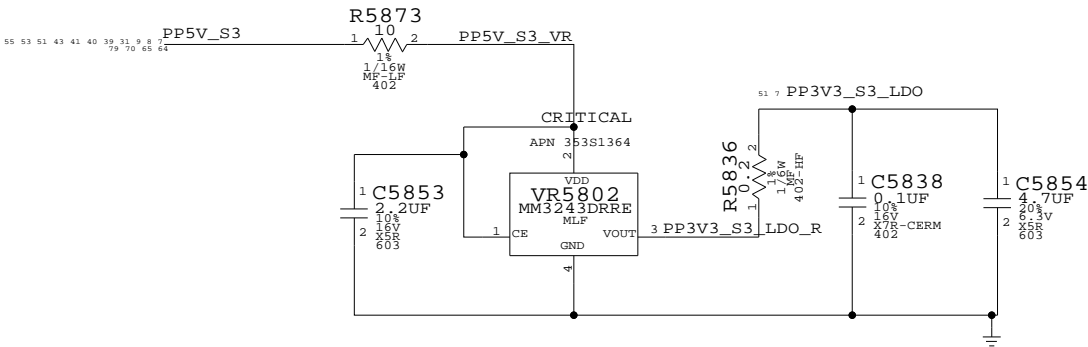
BOOSTER +18.5VDC FOR SENSORS



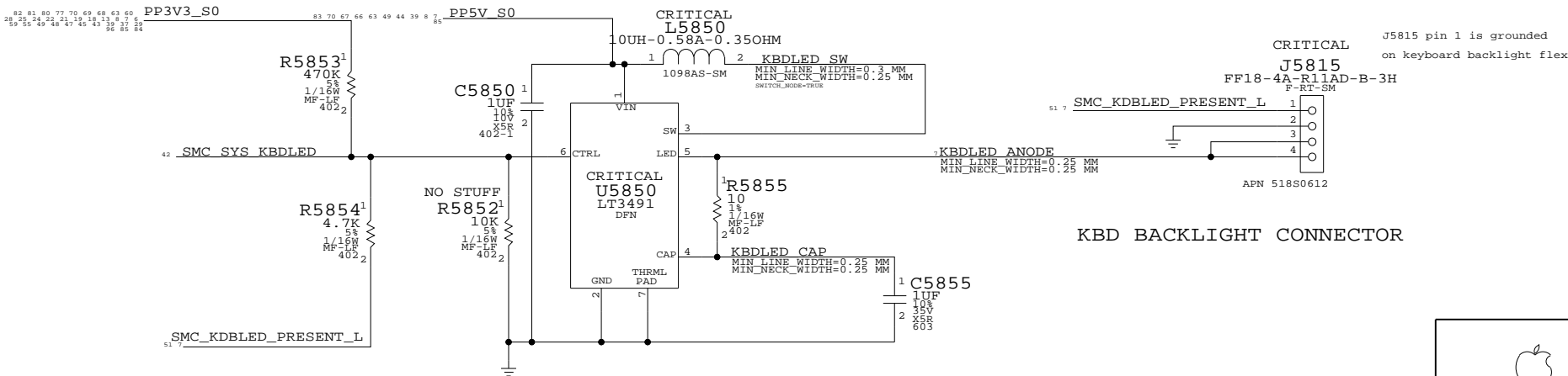
IPD FLEX CONNECTOR



3V3 LDO FOR IPD

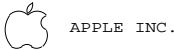


Keyboard LED Driver



KBD BACKLIGHT CONNECTOR

| WELLSPRING 2                                                                                                               |                      |
|----------------------------------------------------------------------------------------------------------------------------|----------------------|
| SYNC_MASTER=PWRSQNC                                                                                                        | SYNC_DATE=01/05/2009 |
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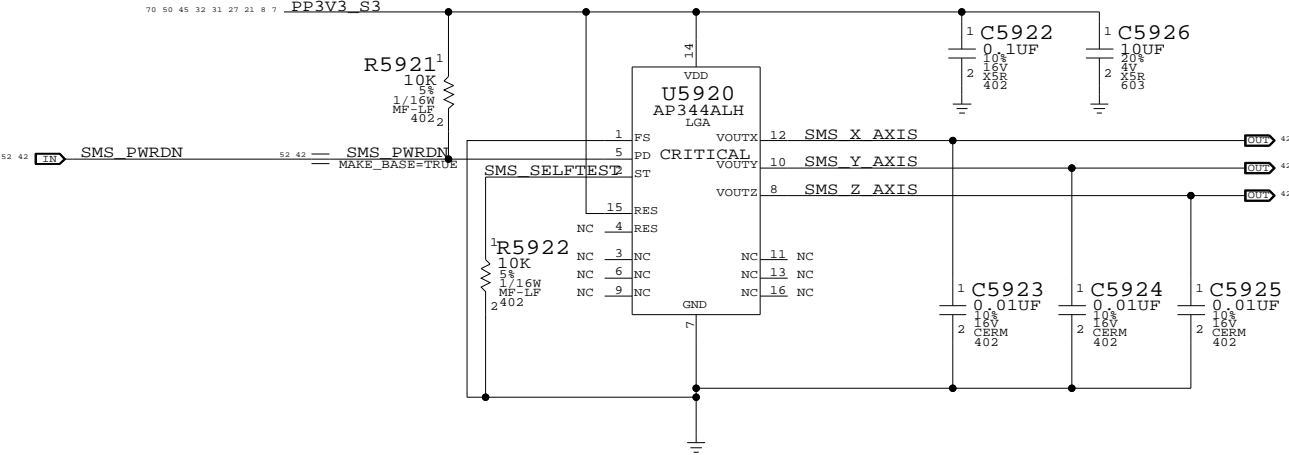
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|-------|----------------|-------|
| D     | 051-7892       | A.0.0 |
| SCALE | SHT            | OF    |
| NONE  | 51             | 97    |

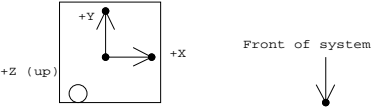


Analog SMS

R5921 PULLS UP SMS\_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:



Circle indicates pin 1 location when placed in correct orientation

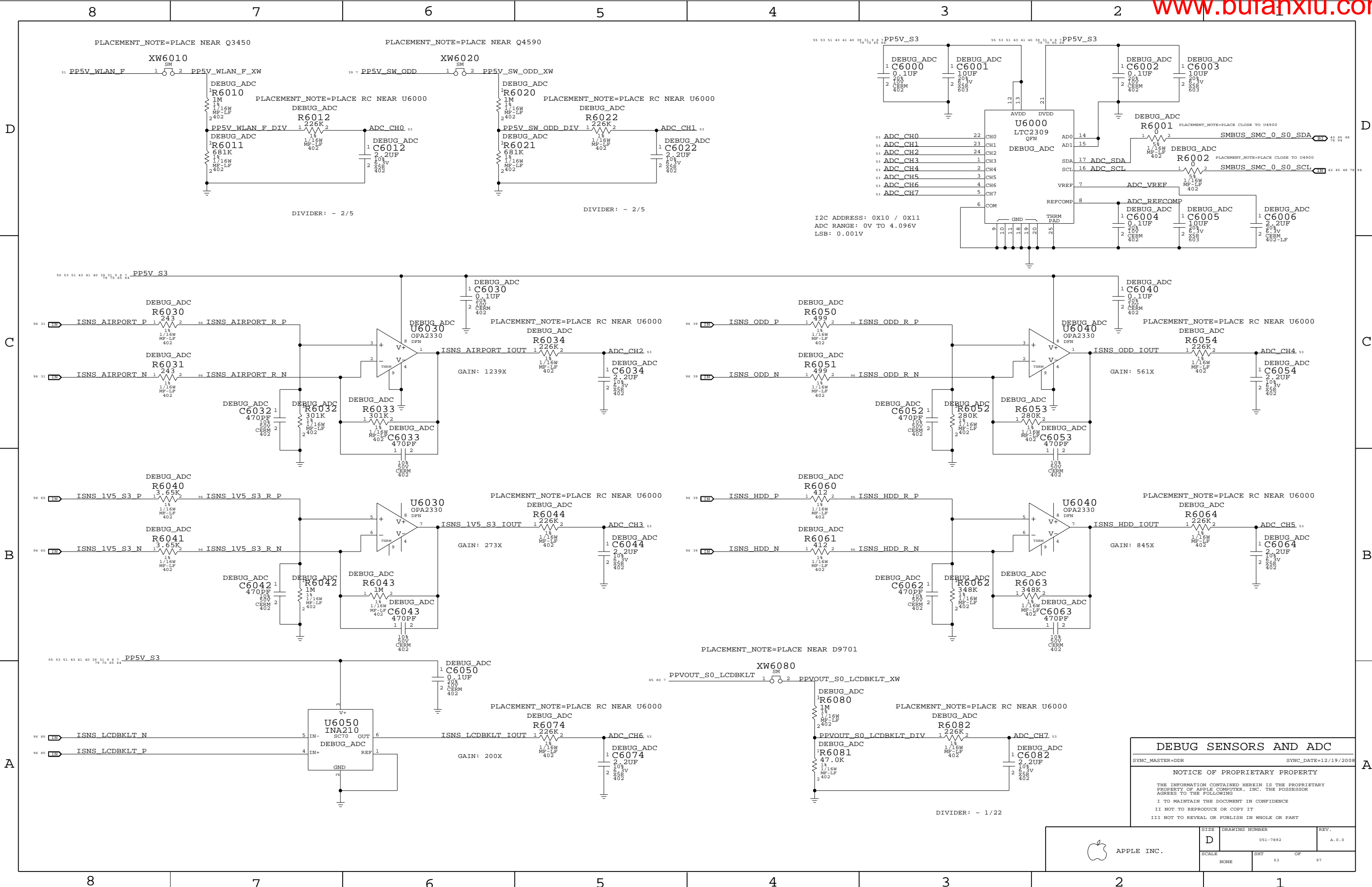
| Sudden Motion Sensor (SMS)                                                                                                 |  |                      |
|----------------------------------------------------------------------------------------------------------------------------|--|----------------------|
| SYNC_MASTER=SENSOR                                                                                                         |  | SYNC_DATE=08/14/2008 |
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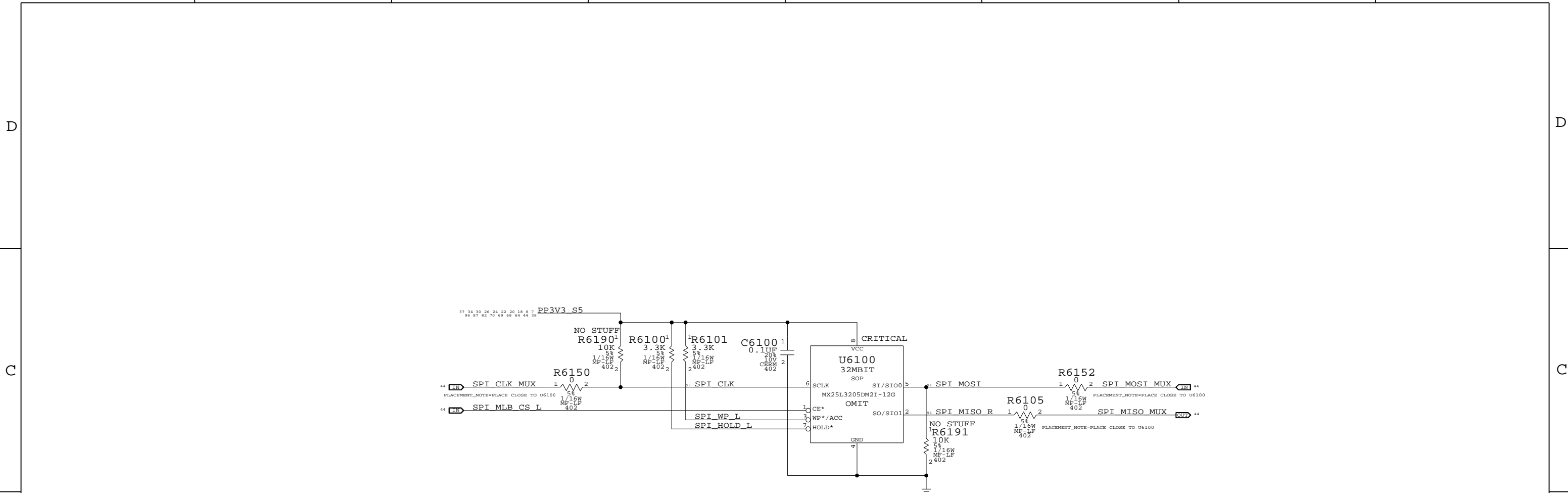
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| D     | 051-7892       | A.0.0 |
| SCALE | SHT            | OF    |
| NONE  | 52             | 97    |









| MCP79 SPI Frequency Select |          |         |
|----------------------------|----------|---------|
| Frequency                  | SPI_MOSI | SPI_CLK |
| 31 MHz                     | 0        | 0       |
| 42 MHz                     | 0        | 1       |
| 25 MHz                     | 1        | 0       |
| 1 MHz                      | 1        | 1       |

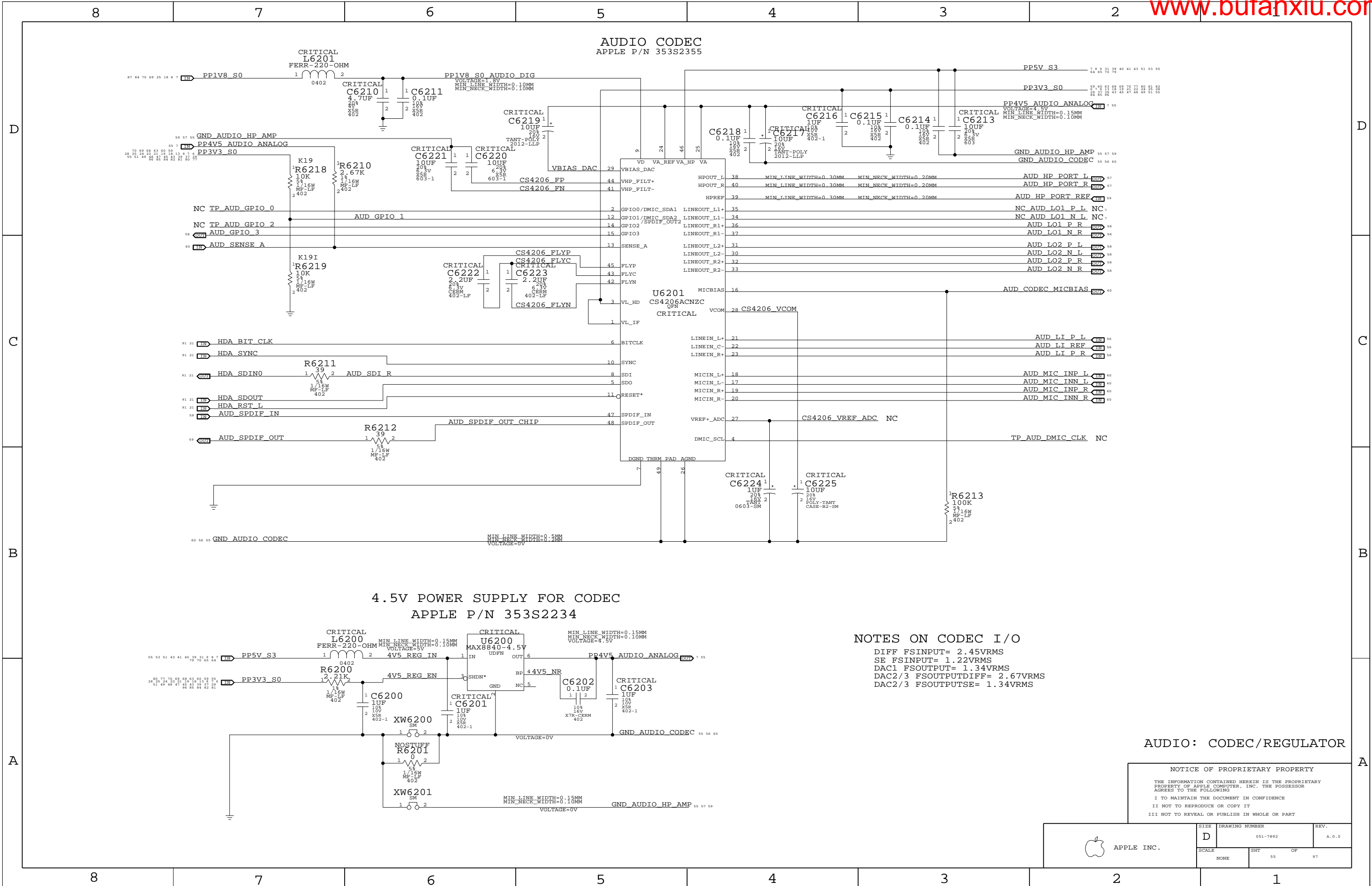
|                                                                                                                          |
|--------------------------------------------------------------------------------------------------------------------------|
| 25MHz is selected with R5190 and R5191<br>Any of the 4 frequencies can be selected<br>with R6190, R6191, R5190 and R5191 |
|--------------------------------------------------------------------------------------------------------------------------|

A

|                                                                                                                            |                      |
|----------------------------------------------------------------------------------------------------------------------------|----------------------|
| SPI ROM                                                                                                                    |                      |
| SYNC_MASTER=CHANG_M98_MLB                                                                                                  | SYNC_DATE=07/01/2008 |
| NOTICE OF PROPRIETARY PROPERTY                                                                                             |                      |
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| III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART                                                                              |                      |

A

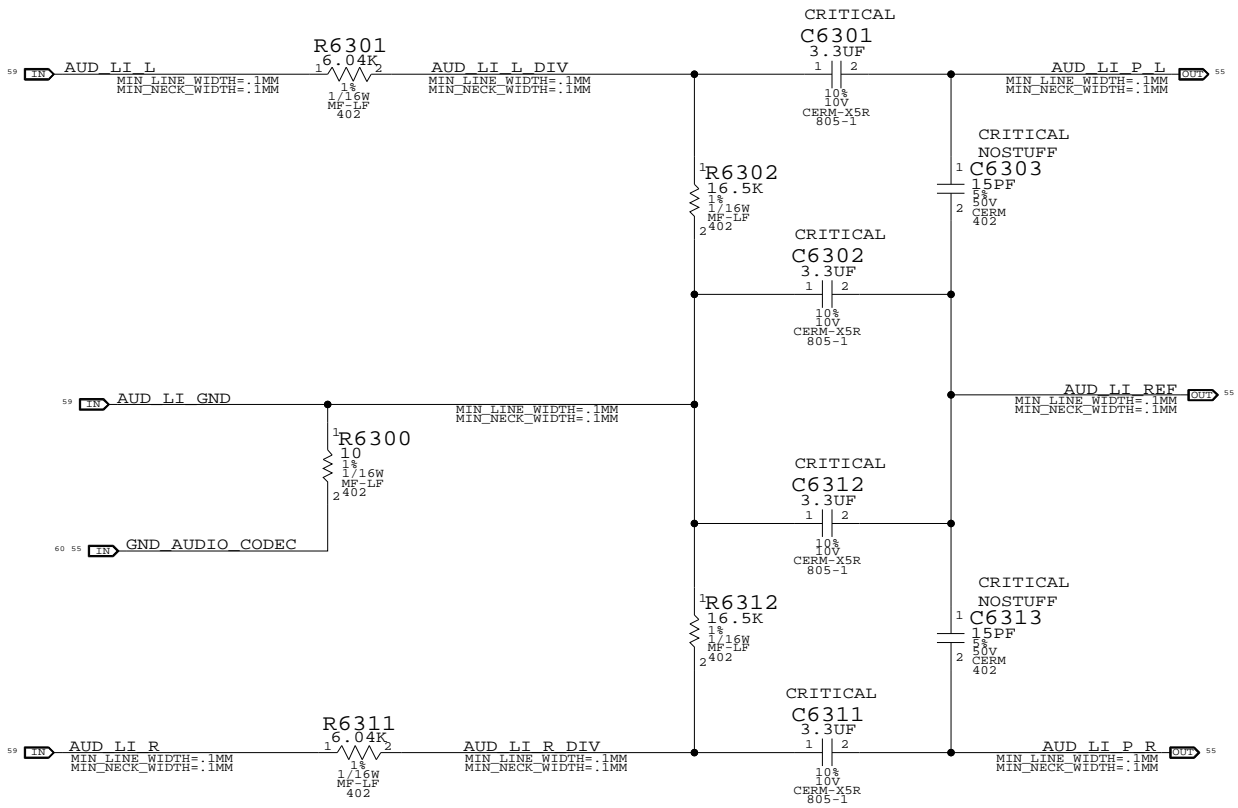






LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS  
NET RIN = 20K OHMS  
FC = 8 HZ  
VIN = 2VRMS, CODEC VIN = 1.21 VRMS



AUDIO: LINE INPUT FILTER

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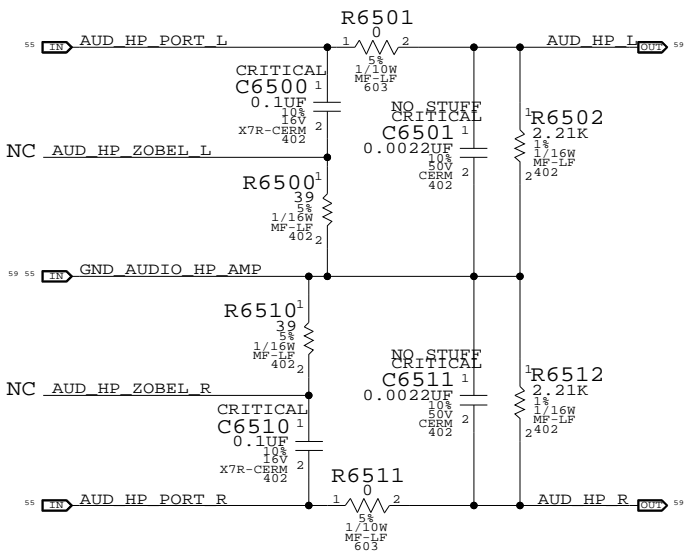


APPLE INC.

| SIZE  | DRAWING NUMBER | REV.  |
|-------|----------------|-------|
| D     | 051-7892       | A.0.0 |
| SCALE | SHT            | OF    |
| NONE  | 56             | 97    |



ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



AUDIO: HEADPHONE FILTER

SYNC\_MASTER=AUDIO SYNC\_DATE=03/16/2009

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| SIZE  | DRAWING NUMBER | REV.  |
|-------|----------------|-------|
| D     | 051-7892       | A.0.0 |
| SCALE | SHT            | OF    |
| NONE  | 57             | 97    |



D

C

B

A

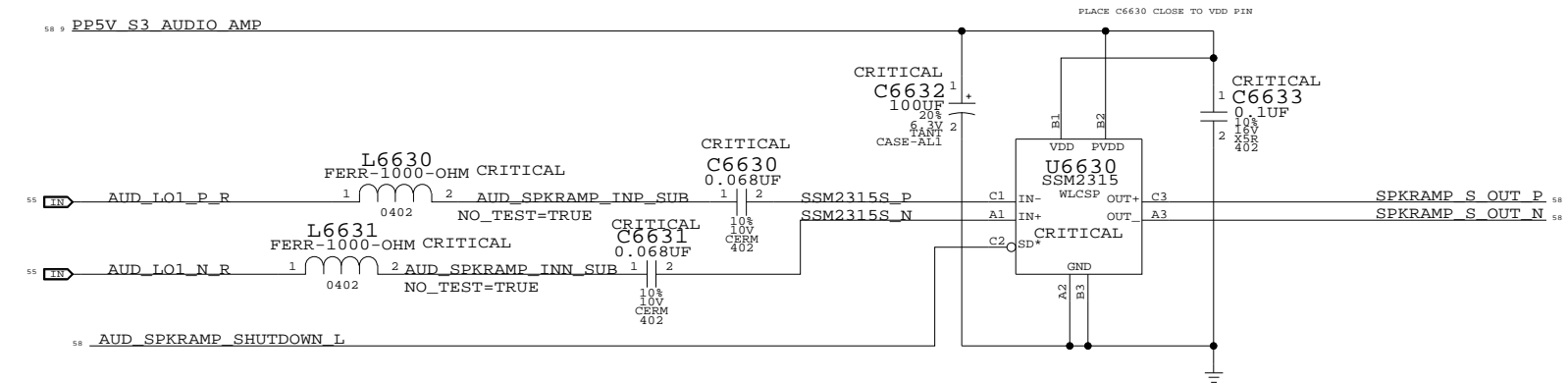
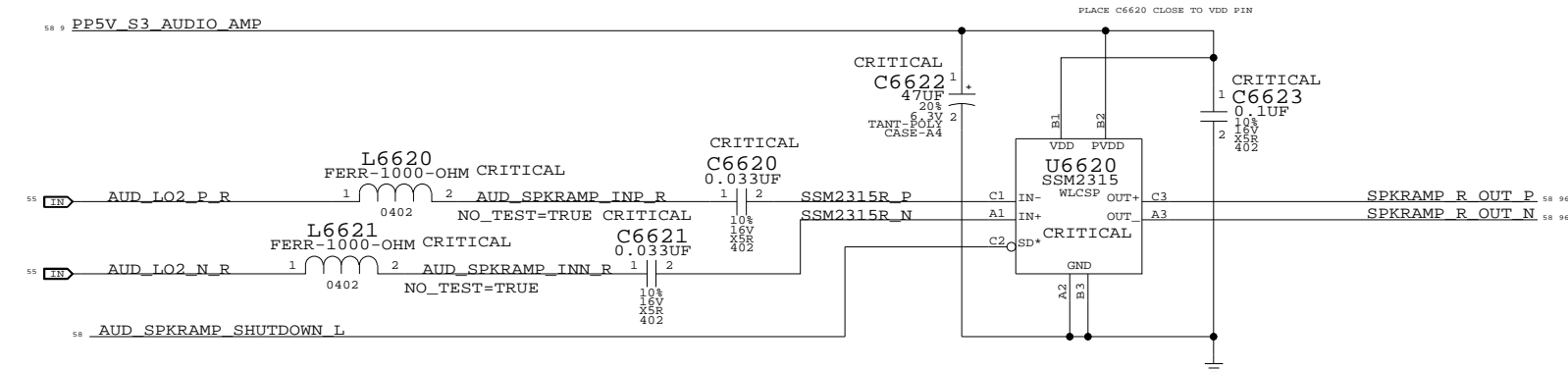
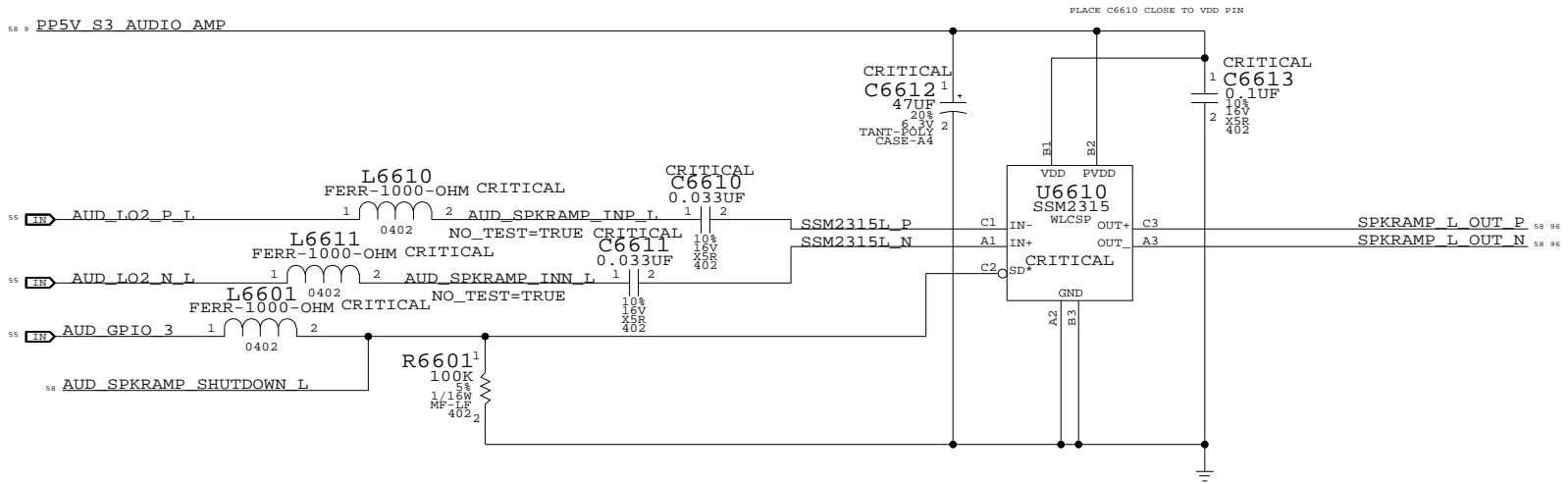
D

C

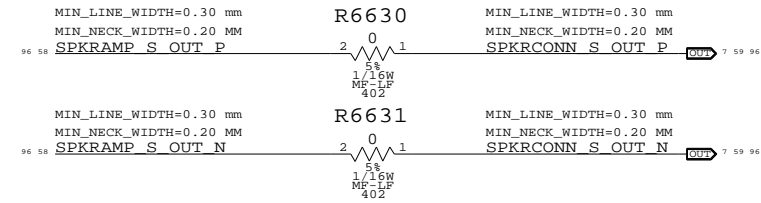
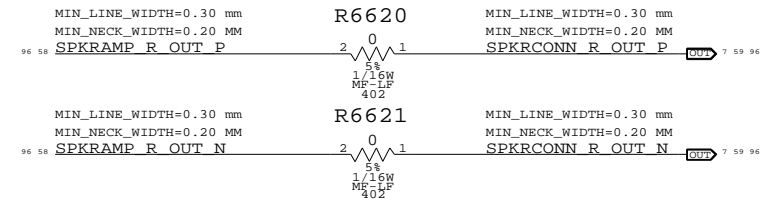
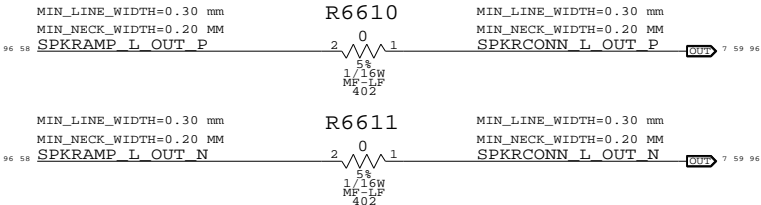
B

A

3X MONO SPEAKER AMPLIFIERS (SSM2315)  
APN: 353S2500  
GAIN = 6DB  
1ST ORDER FC (L&R) = 120 HZ +/- 30%  
1ST ORDER FC (SUB) = 58HZ +/- 30%



SPEAKER CHECKPOINTS

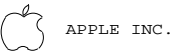


AUDIO: SPEAKER AMP

SYNC\_MASTER=AUDIO SYNC\_DATE=03/16/2009

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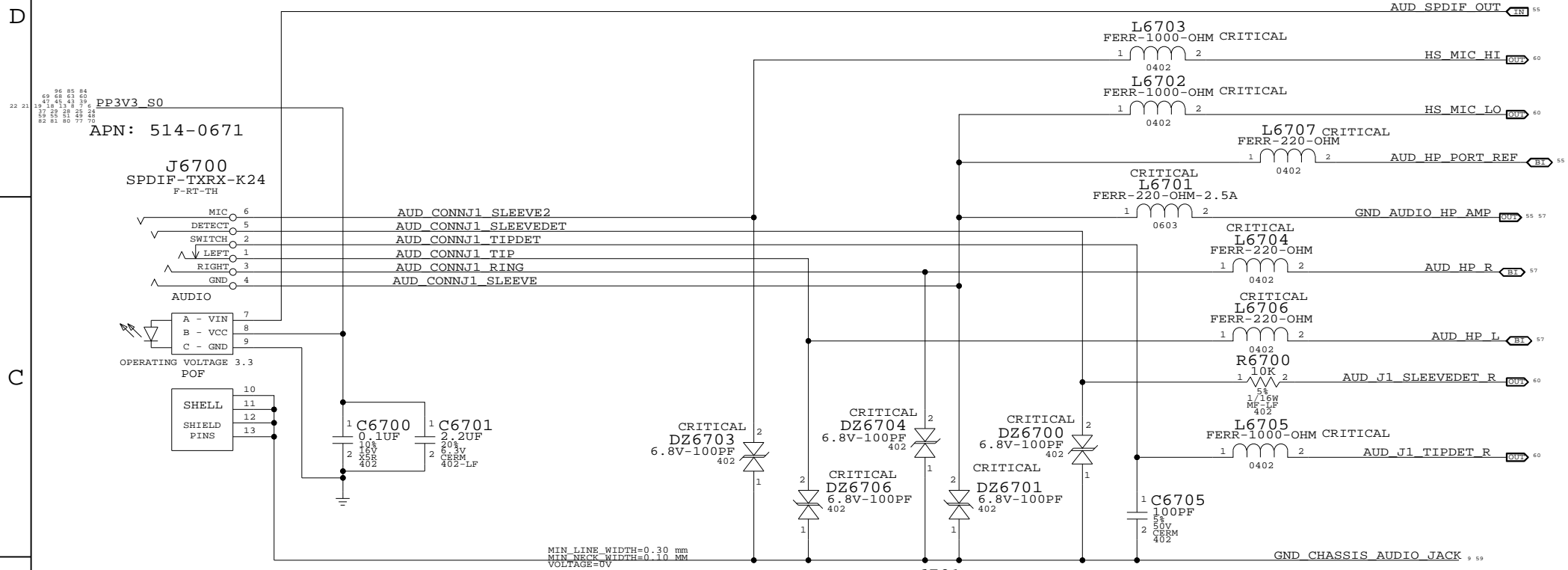


APPLE INC.

| SIZE  | DRAWING NUMBER | REV.  |
|-------|----------------|-------|
| D     | 051-7892       | A.0.0 |
| SCALE | SHT            | OF    |
| NONE  | 58             | 97    |

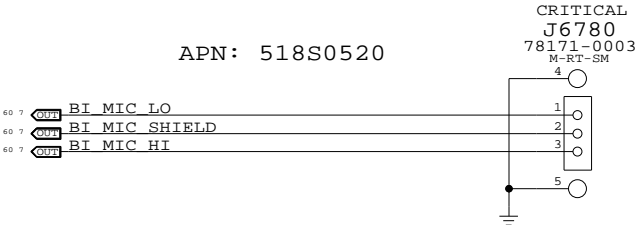


AUDIO JACK 1 LO/HP JACK, SPDIF TX



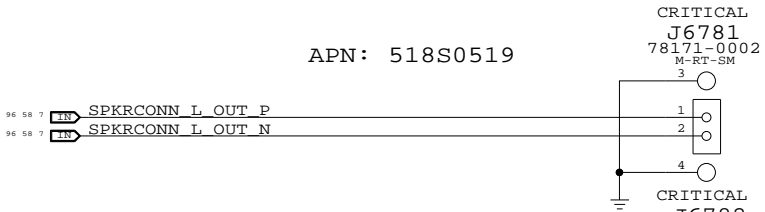
MIC CONNECTOR

APN: 518S0520

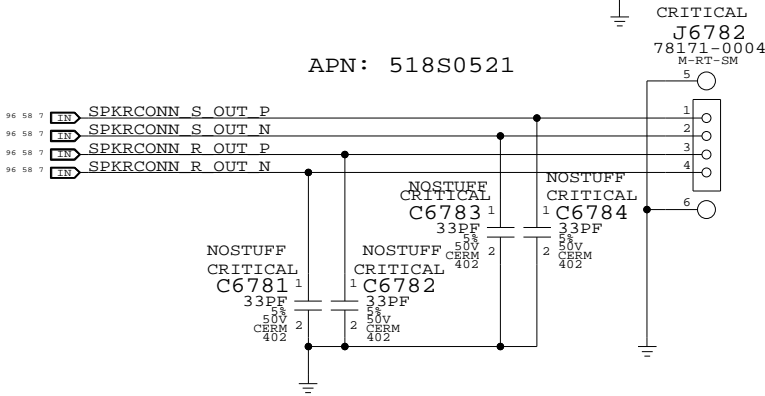


SPEAKER CONNECTOR

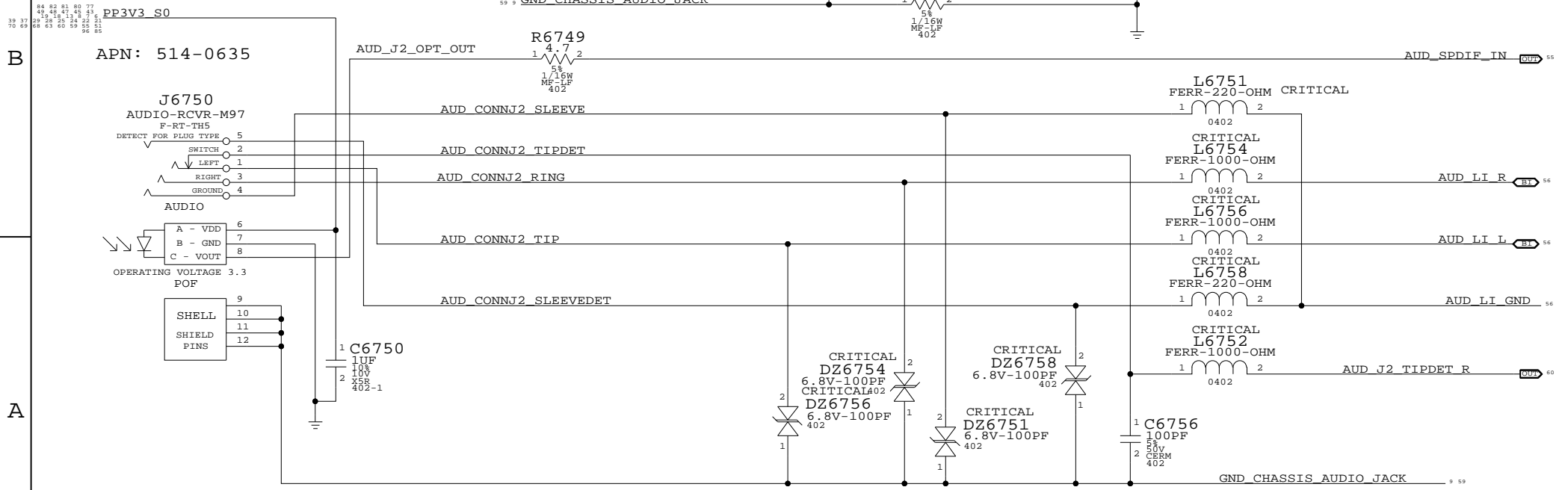
APN: 518S0519



APN: 518S0521



AUDIO JACK 2 LINE IN JACK, SPDIF RX



AUDIO: JACKS

SYNC\_MASTER=AUDIO SYNC\_DATE=03/16/2009

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| SIZE  | DRAWING NUMBER | REV.  |
|-------|----------------|-------|
| D     | 051-7892       | A.0.0 |
| SCALE | SHT            | OF    |
| NONE  | 59             | 97    |



D

C

B

A

D

C

B

A

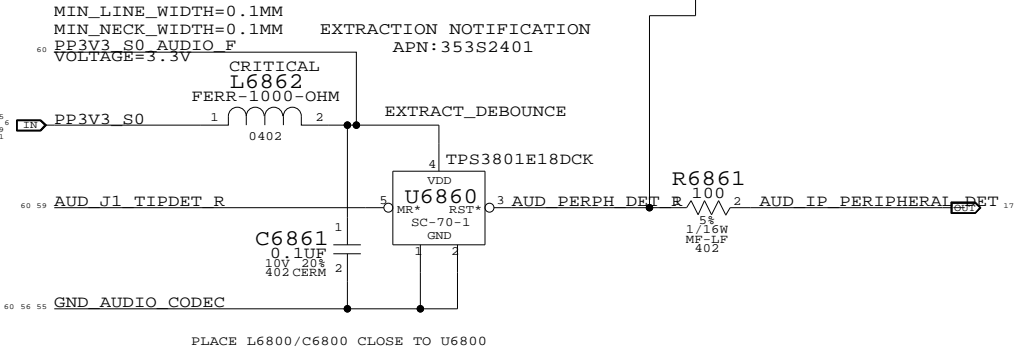
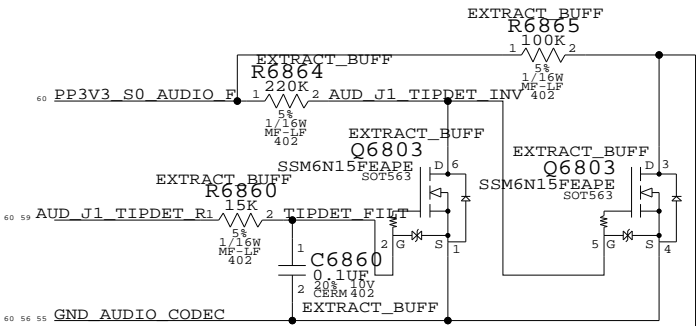
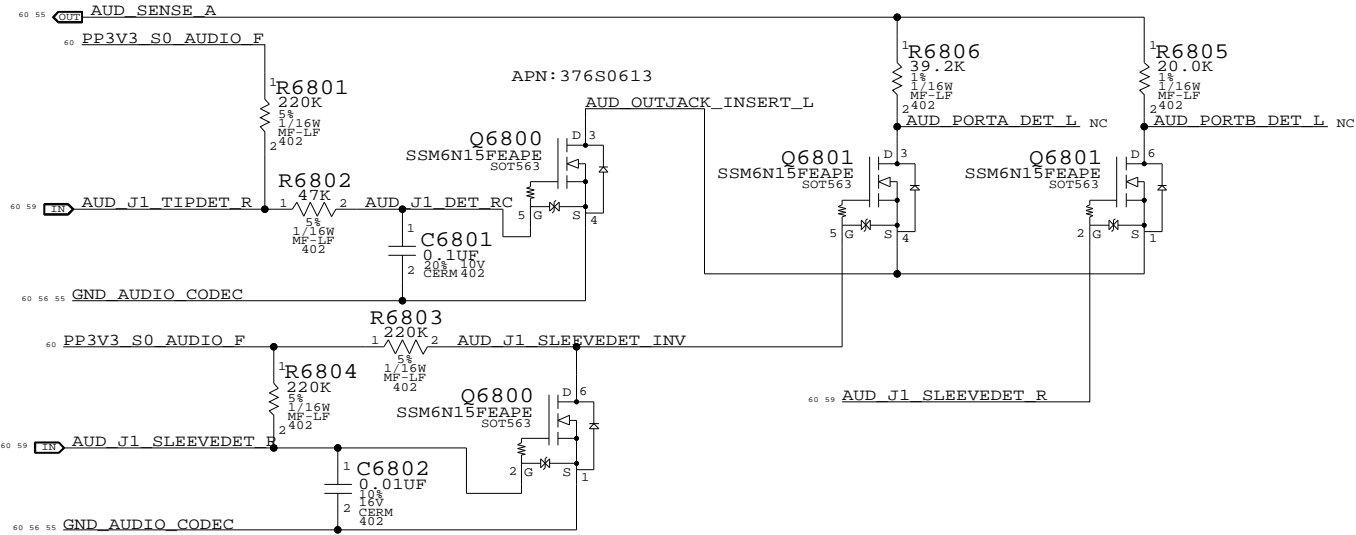
CODEC OUTPUT SIGNAL PATHS

| FUNCTION    | VOLUME   | CONVERTER | PIN COMPLEX | MUTE CONTROL | DET ASSIGNMENT |
|-------------|----------|-----------|-------------|--------------|----------------|
| HP/LINE OUT | 0X02 (2) | 0X02 (2)  | 0X09 (9,A)  | N/A          | 0X09 (A)       |
| SATELLITES  | 0X04 (4) | 0X04 (4)  | 0X0B (11)   | GPIO_3       | N/A            |
| SUB         | 0X03 (3) | 0X03 (03) | 0X0A (10)   | GPIO_3       | N/A            |
| SPDIF OUT   | N/A      | 0X08 (8)  | 0X10 (16)   | N/A          | 0X0C (B)       |

CODEC INPUT SIGNAL PATHS

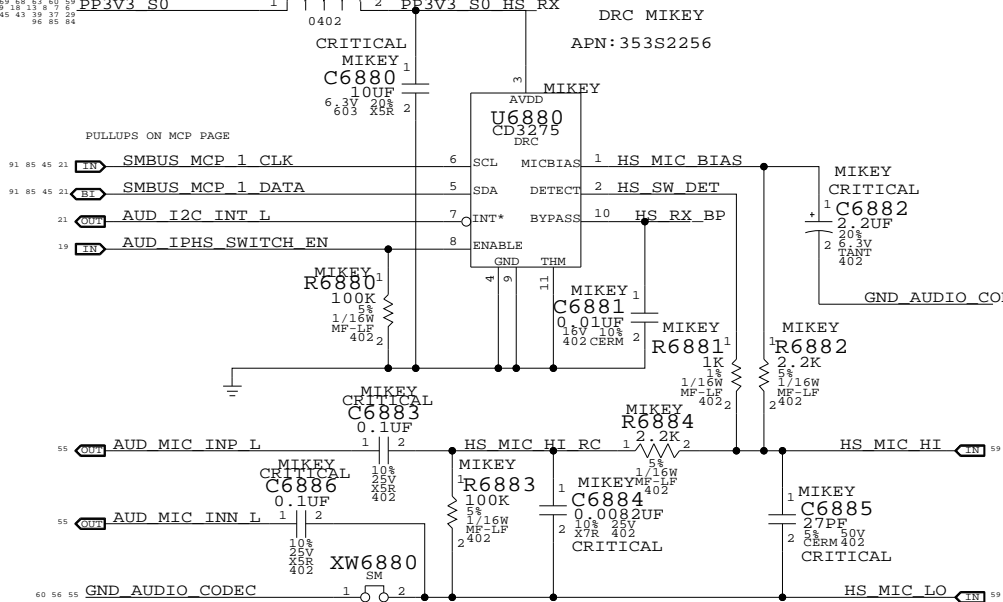
| FUNCTION     | CONVERTER | PIN COMPLEX          | VREF           | DET ASSIGNMENT |
|--------------|-----------|----------------------|----------------|----------------|
| LINE IN      | 0X05 (5)  | 0X0C (12,C)          | N/A            | 0X0C (12,C)    |
| SPDIF IN     | 0X07 (7)  | 0X0F (15)            | N/A            | N/A            |
| BUILT-IN MIC | 0X06 (6)  | 0X0D (13,B,RIGHT)    | MIC_BIAS (80%) | N/A            |
| HEADSET MIC  | 0X06 (6)  | 0X0D (13,V22,B,LEFT) | MIKEY          | MIKEY          |

PORT A DETECT (HEADPHONES) PORT B DETECT (SPDIF DELEGATE)

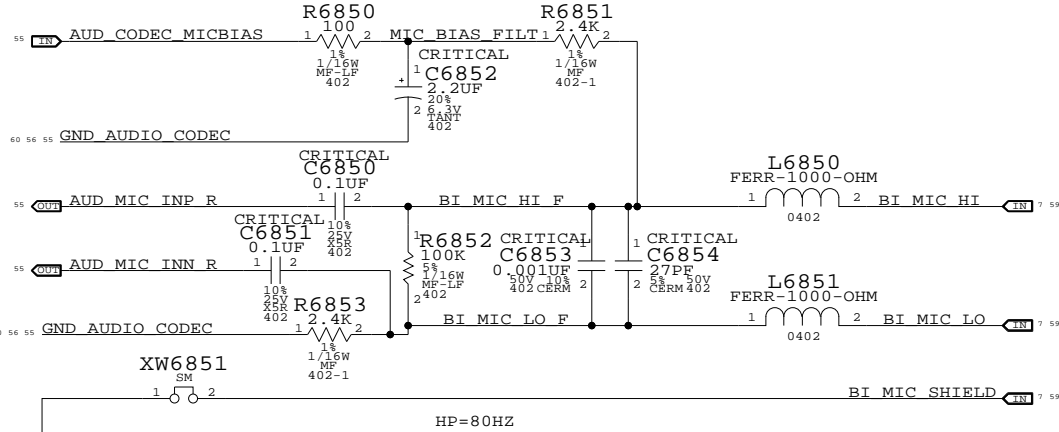


PLACE L6800/C6800 CLOSE TO U6800

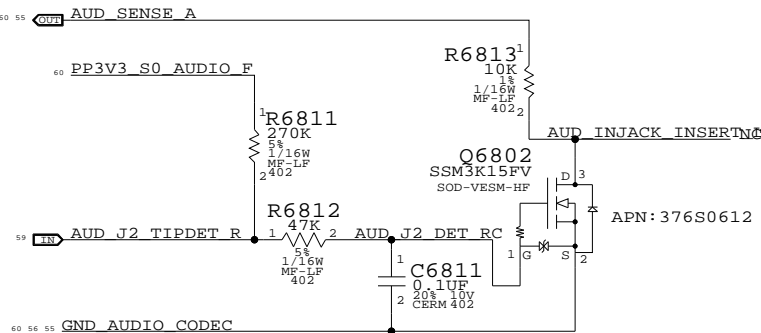
PORT B LEFT(HEADSET MIC)  
CRITICAL HP=80HZ, LP=8.82KHZ  
MIKEY MIN\_LINE\_WIDTH=0.1MM  
L6880 MIN\_NECK\_WIDTH=0.1MM  
FERR-1000-OHM VOLTAGE=3.3V



PORT B RIGHT(BUILT-IN MIC)



PORT C DETECT (LINE-IN)

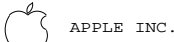


AUDIO: JACK TRANSLATORS

SYNC\_MASTER=AUDIO SYNC\_DATE=03/16/2009

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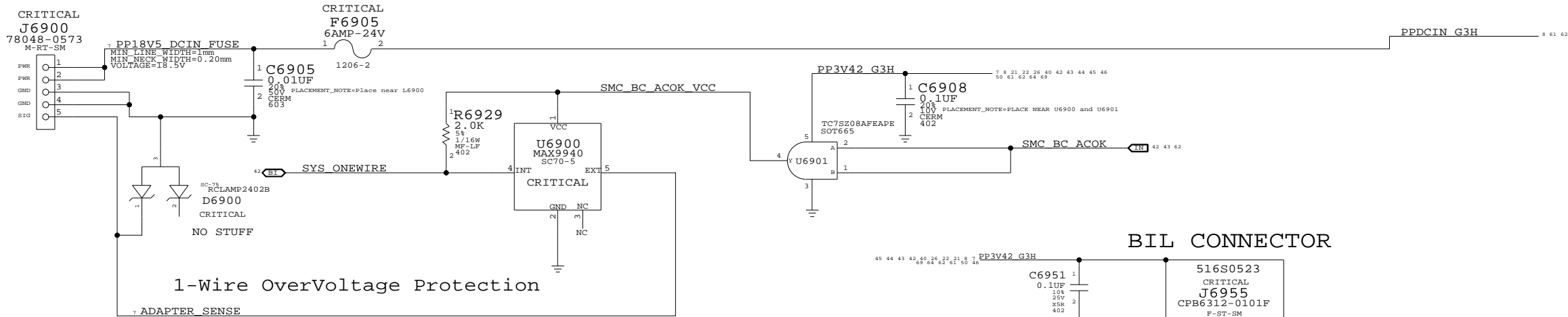
APPLE INC.

SIZE D DRAWING NUMBER 051-7892 REV. A.0.0

SCALE NONE SHT 60 OF 97



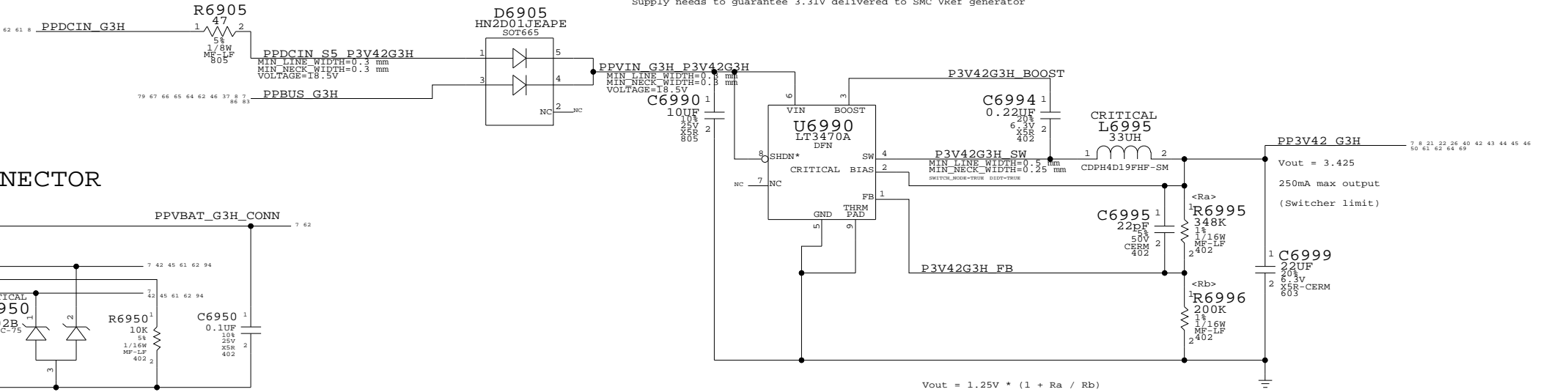
MagSafe DC Power Jack



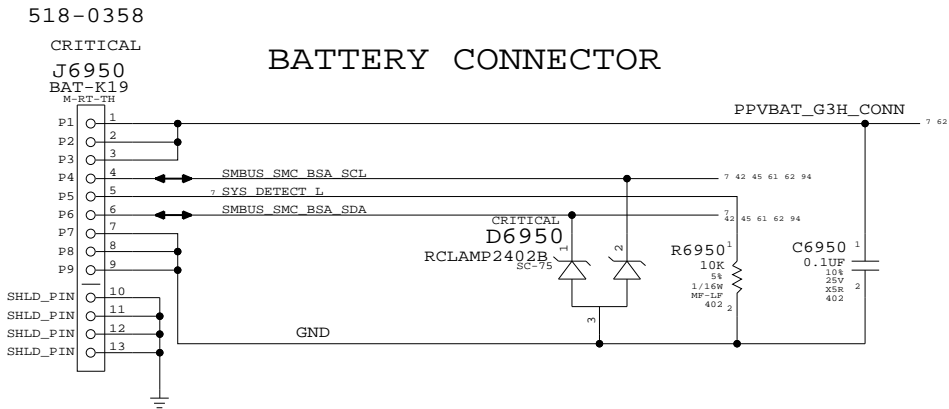
The chassis ground will otherwise float and can send transients onto ADAPTER\_SENSE when AC is connected.

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



DC-In & Battery Connectors

SYNC\_MASTER=YUN\_K19\_MLB SYNC\_DATE=12/16/2008

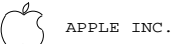
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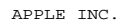
| SIZE  | DRAWING NUMBER | REV.  |
|-------|----------------|-------|
| D     | 051-7892       | A.0.0 |
| SCALE | SHT            | OF    |
| NONE  | 61             | 97    |





```
2S Battery Default
3S Battery Default
```

|               |                            |           |
|---------------|----------------------------|-----------|
| SIZE<br>D     | DRAWING NUMBER<br>051-7892 | REV.<br>A |
| SCALE<br>NONE | SHT<br>62                  | OF<br>97  |



|               |                            |           |
|---------------|----------------------------|-----------|
| SIZE<br>D     | DRAWING NUMBER<br>051-7892 | REV.<br>A |
| SCALE<br>NONE | SHT<br>62                  | OF<br>97  |



www.butanxiu.com

These caps are for Q7100

These caps are for Q7102

| DPRSLPVR | DPRSTP* | PSI* | Operation | Mode |
|----------|---------|------|-----------|------|
| 0        | 1       | 1    | 2-Phase   | CCM  |
| 0        | 1       | 0    | 1-Phase   | CCM  |
| 1        | 0       | 1    | 1-Phase   | DCM  |
| 1        | 0       | 0    | 1-Phase   | DCM  |

Place R7131 Between L7100, L7101 and CPU

IMVP6 CPU VCore Regulator

SYNC\_MASTER=M87\_MLB SYNC\_DATE=10/17/2007

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SIZE D DRAWING NUMBER 051-7892 REV. A.0.0

SCALE NONE SHT 63 OF 97

APPLE INC.





M99 differences from last sync on 11/01/07 to M88 MLB:

1. L7260 changed from M88 MLB inductors to 152S0693.
2. Q7220 changed to 372S0512. Q7225 changed to 376S0511.
3. U7200 changed to 353S2087.
4. Added R7200, R7220, R7221, R7260, R7261, C7201.

100

|       |     |    |
|-------|-----|----|
| SCALE | SHT | OF |
|-------|-----|----|





|       |     |    |
|-------|-----|----|
| SCALE | SHT | OF |
|       | 66  | 03 |







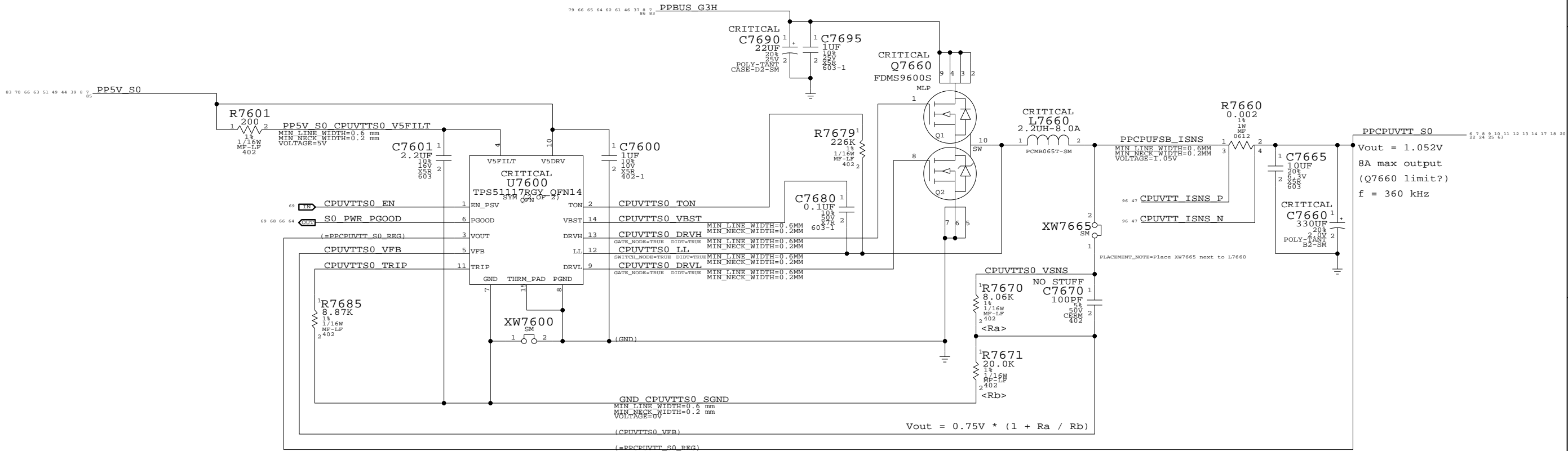
| VID<2:0> | VOLTAGE |
|----------|---------|
| 000      | 1.05V   |
| 001      | 1.00V   |
| 010      | 0.95V   |
| 011      | 0.90V   |
| 100      | 0.85V   |
| 101      | 0.80V   |
| 110      | 0.75V   |
| 111      | 0.70V   |

|   |          |       |
|---|----------|-------|
| D | 051-7892 | A.O.O |
|---|----------|-------|

|       |     |    |
|-------|-----|----|
| SCALE | SHT | OF |
|-------|-----|----|

|       |     |    |
|-------|-----|----|
| SCALE | SHT | OF |
|-------|-----|----|





M99 differences from last sync on 12/03/07 to T18 MLB:  
1. Tied THERMAL\_PAD to PGND. GND and THERMAL\_PAD disconnected.

CPU VTT / 1V05 S0 Power Supply

SYNC\_MASTER=M99\_MLB SYNC\_DATE=12/14/2007

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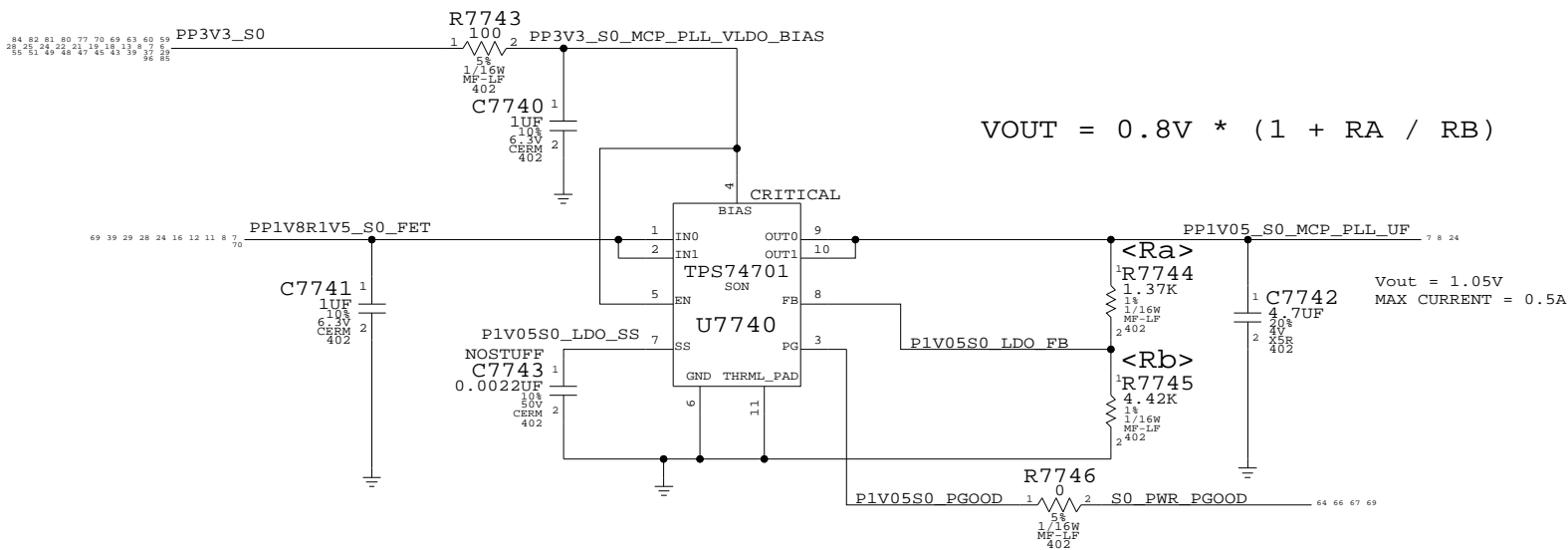


APPLE INC.

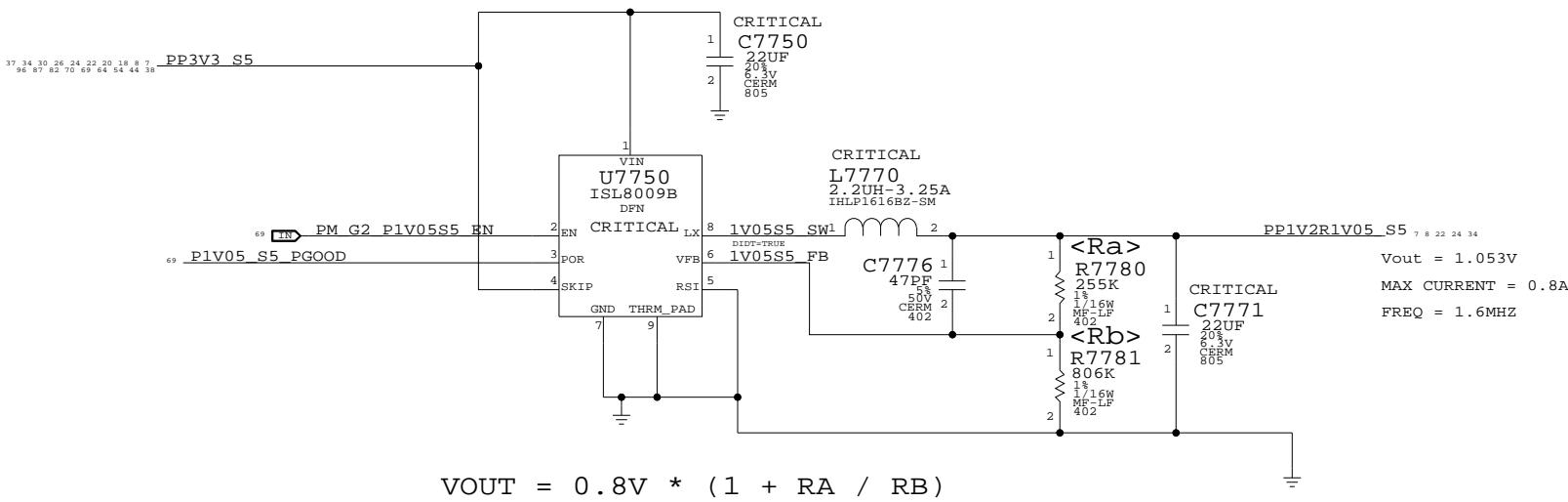
| SIZE  | DRAWING NUMBER | REV.  |
|-------|----------------|-------|
| D     | 051-7892       | A.0.0 |
| SCALE | SHT            | OF    |
| NONE  | 67             | 97    |



1.05V S0 PLL LDO



MCP 1.05V S5 (AUXC) SUPPLY



Misc Power Supplies

SYNC\_MASTER=M99\_MLS SYNC\_DATE=12/14/2007

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SIZE

D

SCALE

NONE

DRAWING NUMBER

051-7892

REV.

A.0.0

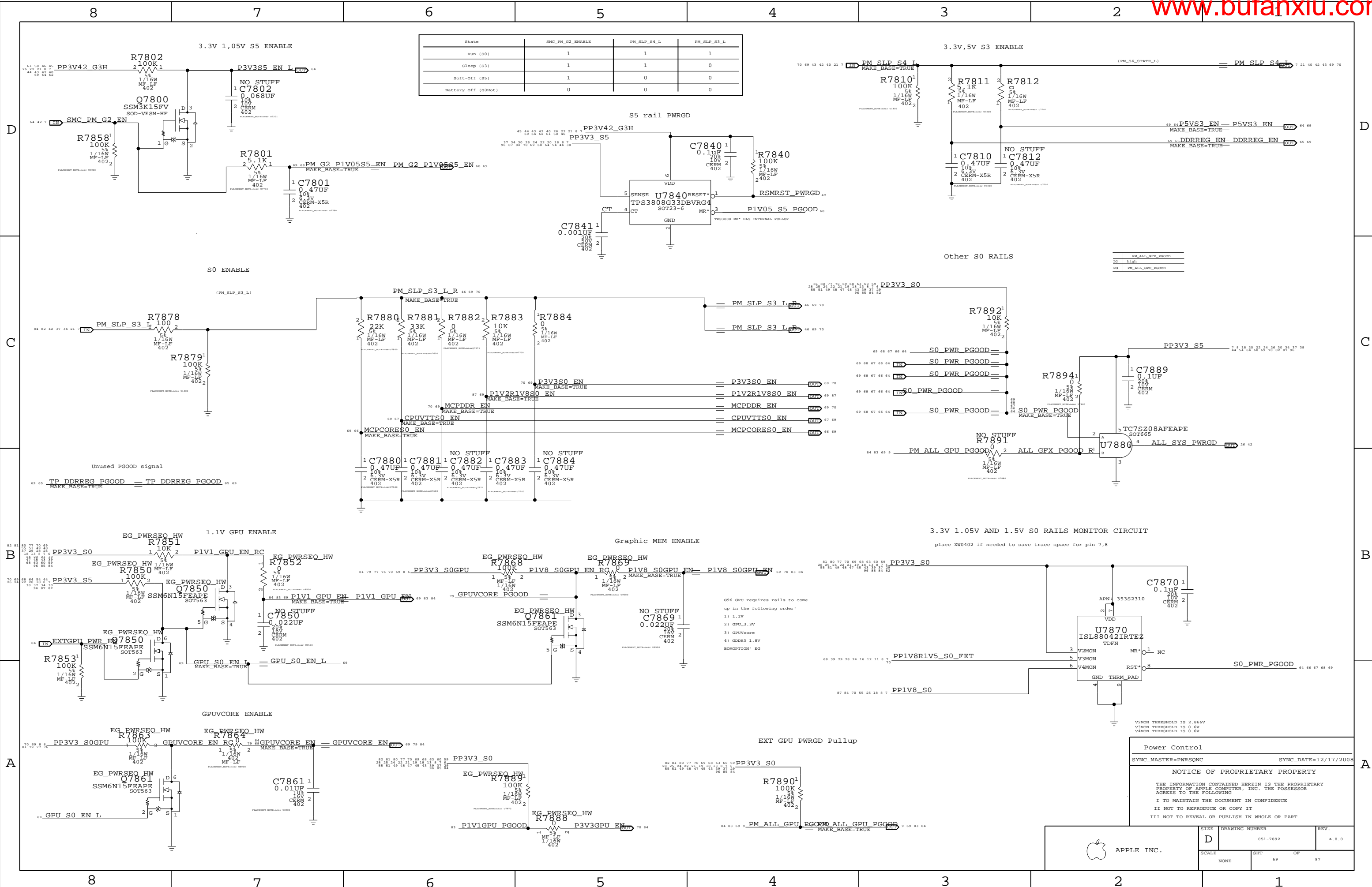
SHT

OF

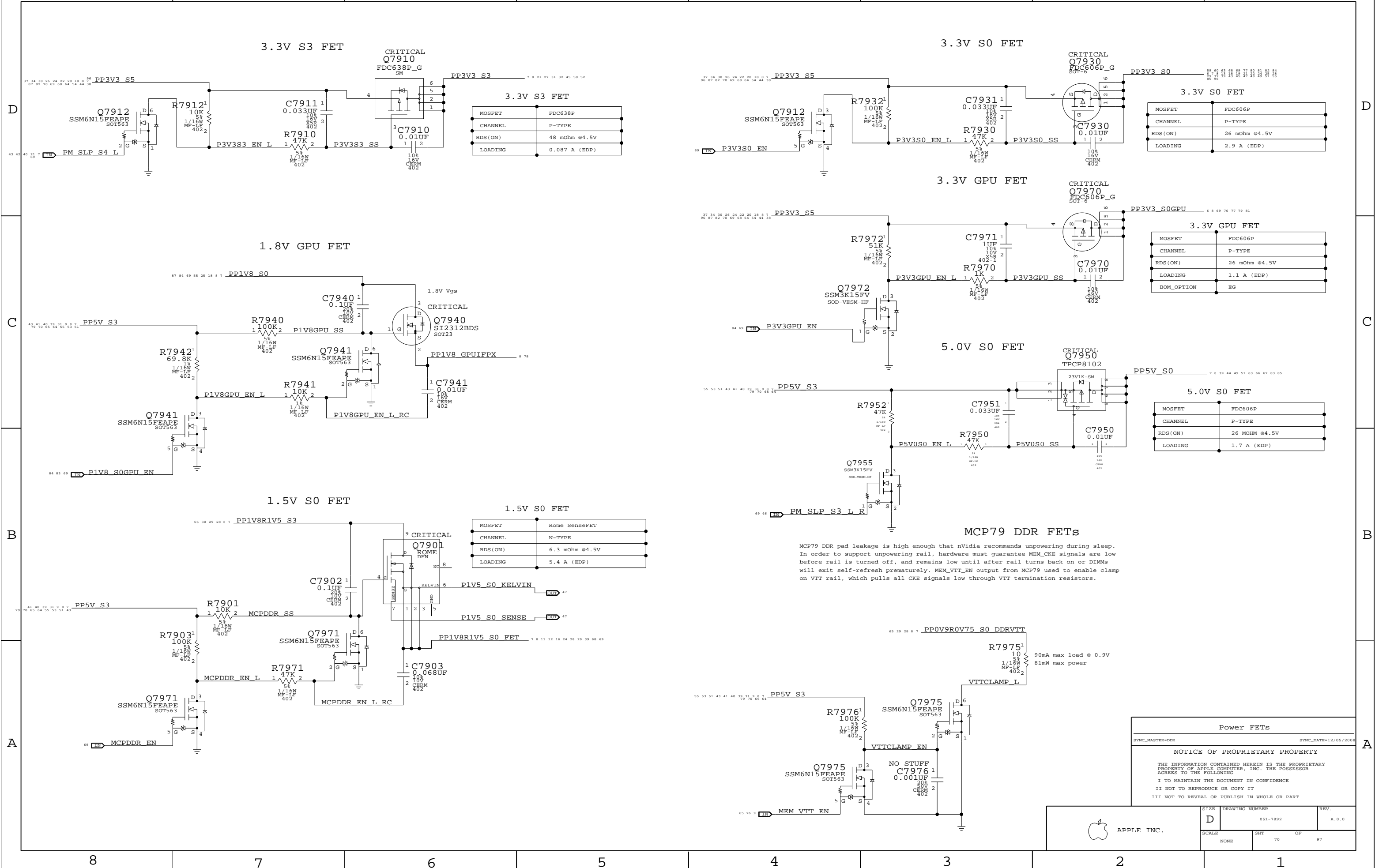
68

97











Power aliases required by this page:

- =PPlV2\_GPU\_PEX\_PL1XVDD
- =PPlV2\_GPU\_PEX\_IOVDDQ
- =PPlV2\_GPU\_PEX\_IOVDD

---

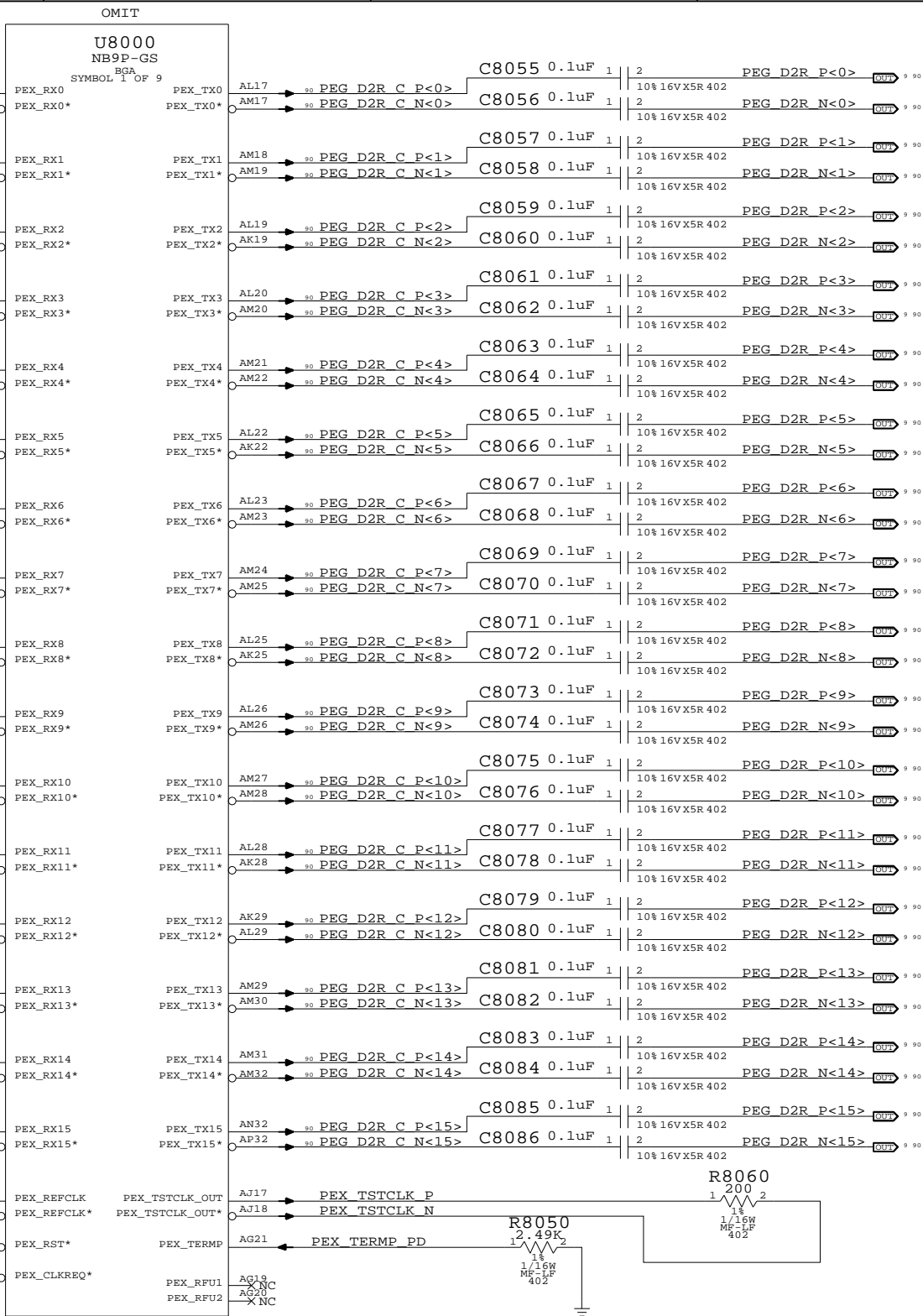
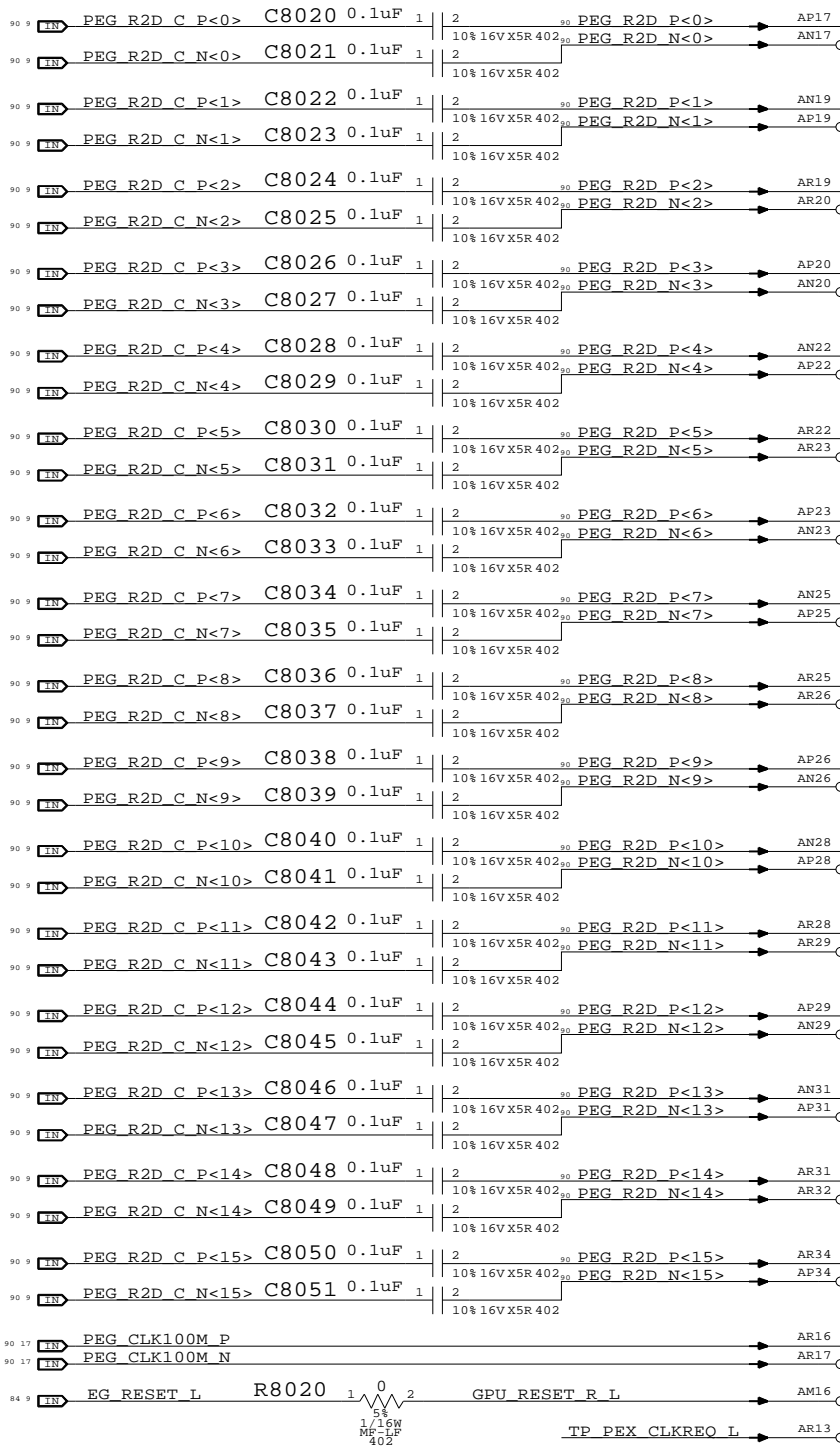
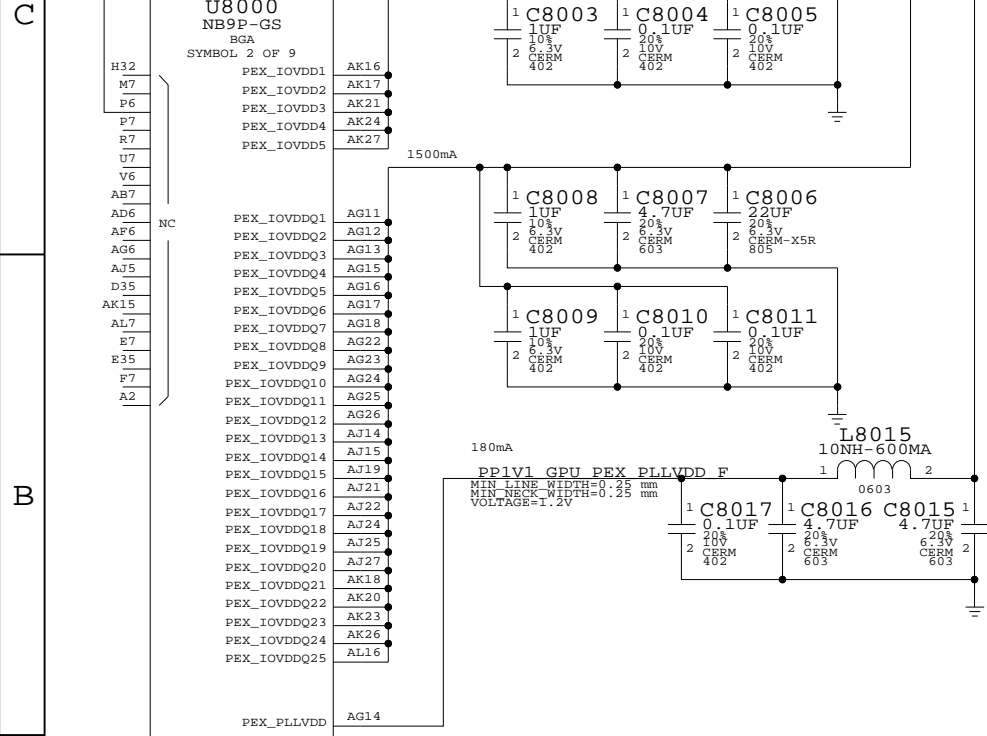
Signal aliases required by this page:

(NONE)

---

BOM options provided by this page:

(NONE)



```

NV G96 PCI-E
SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008
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|               |                            |           |
|---------------|----------------------------|-----------|
| SIZE<br>D     | DRAWING NUMBER<br>051-7892 | REV.<br>A |
| SCALE<br>NONE | SHT<br>71                  | OF<br>97  |



Page Notes

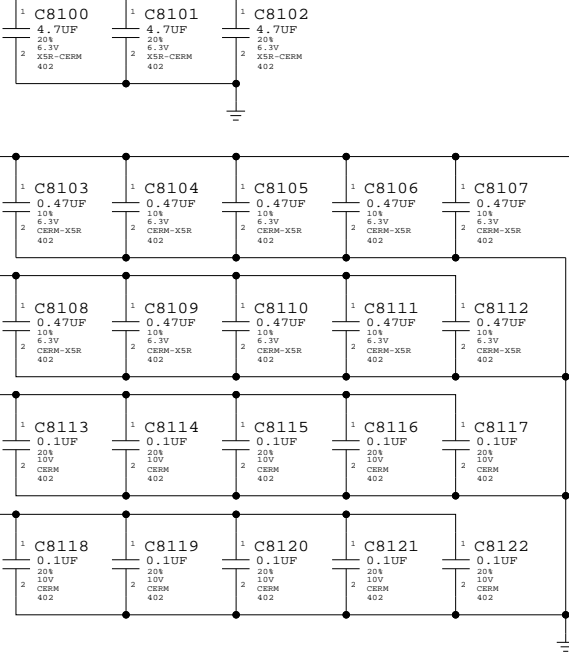
Power aliases required by this page:  
- =PPVCORE\_GPU  
- =PP1V8\_GPU\_FBVDDQ

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

79 PPVCORE\_GPU

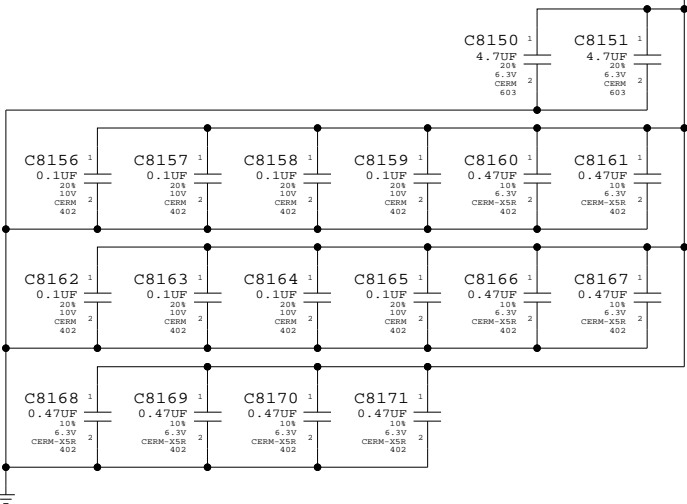
???A @ ???MHz Core/Mem Clk for VDD



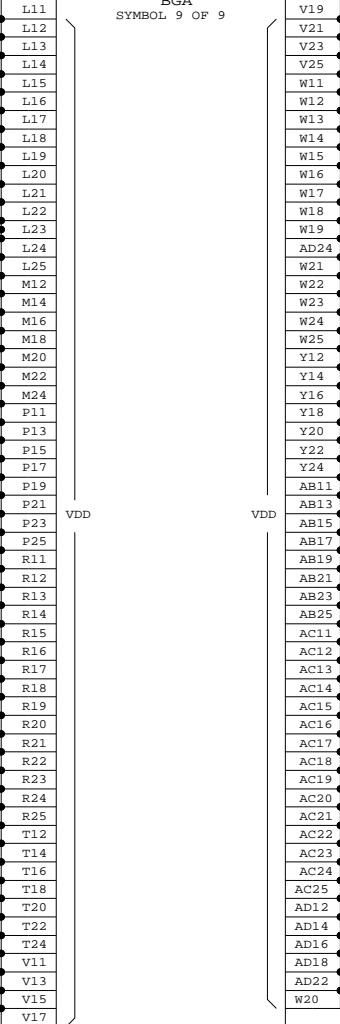
75 74 73 47 9 8 PP1V8\_S0GPU\_ISNS

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

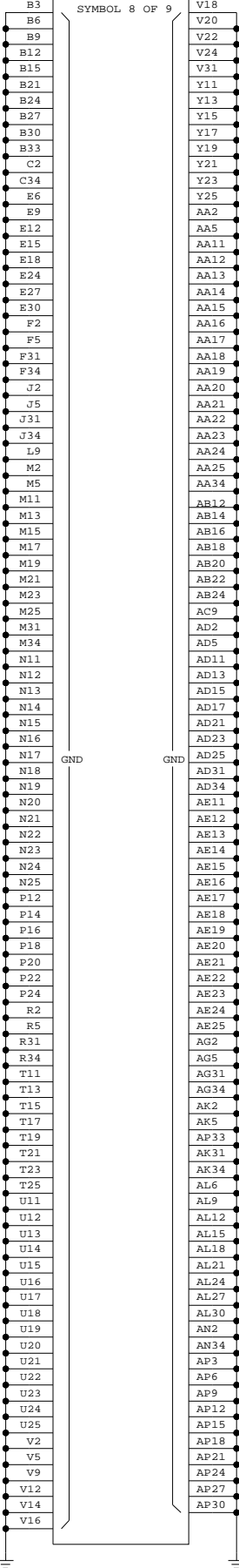
???A @ ???MHz 1.8V GDDR3



U8000  
NB9P-GS  
BGA  
SYMBOL 9 OF 9



U8000  
NB9P-GS  
BGA  
SYMBOL 8 OF 9

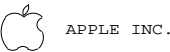


NV G96 Core/FB Power

SYNC\_MASTER=MUXGFX SYNC\_DATE=07/10/2008

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|-------|----------------|-------|
| D     | 051-7892       | A.0.0 |
| SCALE | SHT            | OF    |
| NONE  | 72             | 97    |



Page Notes

Power aliases required by this page:  
- =PP1V2\_GPU\_FBPLLAVDD  
- =PP1V8\_GPU\_FBIO

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

OMIT

U8000  
NB9P-GS  
BGA  
SYMBOL 3 OF 9

|                 |      |                |  |
|-----------------|------|----------------|--|
| FBA_CMD0        | V32  | FB A LMA<4>    |  |
| FBA_CMD1        | W31  | FB A RAS L     |  |
| FBA_CMD2        | U31  | FB A LMA<5>    |  |
| FBA_CMD3        | Y32  | FB A BA<1>     |  |
| FBA_CMD5        | AB35 | FB A UMA<2>    |  |
| FBA_CMD6        | AB34 | FB A UMA<4>    |  |
| FBA_CMD7        | W35  | FB A UMA<3>    |  |
| FBA_CMD7        | W33  | NC FB A CS1 L  |  |
| FBA_CMD8        | W30  | FB A CS0 L     |  |
| FBA_CMD9        | T34  | FB A MA<11>    |  |
| FBA_CMD10       | T35  | FB A CAS L     |  |
| FBA_CMD11       | AB31 | FB A WE L      |  |
| FBA_CMD12       | Y30  | FB A BA<0>     |  |
| FBA_CMD13       | Y34  | FB A UMA<5>    |  |
| FBA_CMD14       | W32  | FB A MA<12>    |  |
| FBA_CMD15       | AA30 | FB A DRAM RST  |  |
| FBA_CMD16       | AA32 | FB A MA<7>     |  |
| FBA_CMD17       | Y33  | FB A MA<10>    |  |
| FBA_CMD18       | U32  | FB A CKE       |  |
| FBA_CMD19       | Y31  | FB A MA<0>     |  |
| FBA_CMD20       | U34  | FB A MA<9>     |  |
| FBA_CMD21       | Y35  | FB A MA<6>     |  |
| FBA_CMD22       | W34  | FB A LMA<2>    |  |
| FBA_CMD23       | V30  | FB A MA<8>     |  |
| FBA_CMD24       | U35  | FB A LMA<3>    |  |
| FBA_CMD25       | U30  | FB A MA<1>     |  |
| FBA_CMD26       | U33  | NC FBA MA<13>  |  |
| FBA_CMD27       | AB30 | FB A BA<2>     |  |
| FBA_CMD28       | AB33 | NC FBA CMD28   |  |
| FBA_CMD29       | T33  | NC FBA CMD29   |  |
| FBA_CMD30       | W29  | NC FBA CMD30   |  |
| FBA_CLK0        | T32  | FB A CLK P<0>  |  |
| FBA_CLK0*       | T31  | FB A CLK N<0>  |  |
| FBA_CLK1        | AC31 | FB A CLK P<1>  |  |
| FBA_CLK1*       | AC30 | FB A CLK N<1>  |  |
| FBA_DQM0        | P30  | FB A DQM L<0>  |  |
| FBA_DQM1        | P32  | FB A DQM L<1>  |  |
| FBA_DQM2        | J30  | FB A DQM L<2>  |  |
| FBA_DQM3        | H34  | FB A DQM L<3>  |  |
| FBA_DQM4        | AF32 | FB A DQM L<4>  |  |
| FBA_DQM5        | AF35 | FB A DQM L<5>  |  |
| FBA_DQM6        | AL32 | FB A DQM L<6>  |  |
| FBA_DQM7        | AL34 | FB A DQM L<7>  |  |
| FBA_DQS_RN0     | N32  | FB A RDQS<0>   |  |
| FBA_DQS_RN1     | L35  | FB A RDQS<1>   |  |
| FBA_DQS_RN2     | H31  | FB A RDQS<2>   |  |
| FBA_DQS_RN3     | G35  | FB A RDQS<3>   |  |
| FBA_DQS_RN4     | AD32 | FB A RDQS<4>   |  |
| FBA_DQS_RN5     | AC34 | FB A RDQS<5>   |  |
| FBA_DQS_RN6     | AJ31 | FB A RDQS<6>   |  |
| FBA_DQS_RN7     | AJ35 | FB A RDQS<7>   |  |
| FBA_DQS_WP0     | N31  | FB A WDQS<0>   |  |
| FBA_DQS_WP1     | L34  | FB A WDQS<1>   |  |
| FBA_DQS_WP2     | J32  | FB A WDQS<2>   |  |
| FBA_DQS_WP3     | H35  | FB A WDQS<3>   |  |
| FBA_DQS_WP4     | AE31 | FB A WDQS<4>   |  |
| FBA_DQS_WP5     | AC33 | FB A WDQS<5>   |  |
| FBA_DQS_WP6     | AJ32 | FB A WDQS<6>   |  |
| FBA_DQS_WP7     | AJ34 | FB A WDQS<7>   |  |
| FB_DLLAVDD0     | AG27 |                |  |
| FB_PLLAVDD0     | AF27 |                |  |
| FBA_DEBUG       | T30  | FBA DEBUG      |  |
| FB_CAL_PD_VDDQ  | K27  | FBCAL PD VDDQ  |  |
| FB_CAL_PU_GND   | L27  | FBCAL PU GND   |  |
| FB_CAL_TERM_GND | M27  | FBCAL TERM GND |  |

PLACEMENT\_NOTE=Place close to U8000.

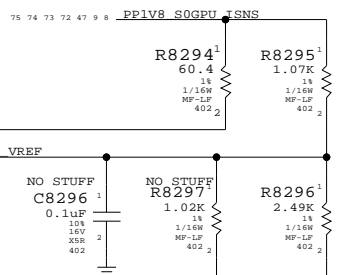
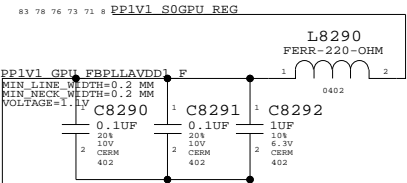
PLACEMENT\_NOTE=Place close to U8000.

PLACEMENT\_NOTE=Place close to U8000.

OMIT

U8000  
NB9P-GS  
BGA  
SYMBOL 4 OF 9

|             |     |               |  |
|-------------|-----|---------------|--|
| FBC_CMD0    | C17 | FB B LMA<4>   |  |
| FBC_CMD1    | B19 | FB B RAS L    |  |
| FBC_CMD2    | D18 | FB B LMA<5>   |  |
| FBC_CMD3    | F21 | FB B BA<1>    |  |
| FBC_CMD4    | A23 | FB B UMA<2>   |  |
| FBC_CMD5    | D21 | FB B UMA<4>   |  |
| FBC_CMD6    | B23 | FB B UMA<3>   |  |
| FBC_CMD7    | E20 | NC FB B CS1 L |  |
| FBC_CMD8    | G21 | FB B CS0 L    |  |
| FBC_CMD9    | F19 | FB B MA<11>   |  |
| FBC_CMD10   | F20 | FB B CAS L    |  |
| FBC_CMD11   | F23 | FB B WE L     |  |
| FBC_CMD12   | A22 | FB B BA<0>    |  |
| FBC_CMD13   | C22 | FB B UMA<5>   |  |
| FBC_CMD14   | B17 | FB B MA<12>   |  |
| FBC_CMD15   | F24 | FB B DRAM RST |  |
| FBC_CMD16   | C25 | FB B MA<7>    |  |
| FBC_CMD17   | E22 | FB B MA<10>   |  |
| FBC_CMD18   | C20 | FB B CKE      |  |
| FBC_CMD19   | B22 | FB B MA<0>    |  |
| FBC_CMD20   | A19 | FB B MA<9>    |  |
| FBC_CMD21   | D22 | FB B MA<6>    |  |
| FBC_CMD22   | D20 | FB B LMA<2>   |  |
| FBC_CMD23   | E19 | FB B MA<8>    |  |
| FBC_CMD24   | D19 | FB B LMA<3>   |  |
| FBC_CMD25   | F18 | FB B MA<1>    |  |
| FBC_CMD26   | C19 | NC FBB MA<13> |  |
| FBC_CMD27   | F22 | FB B BA<2>    |  |
| FBC_CMD28   | C23 | NC FBC CMD28  |  |
| FBC_CMD29   | B20 | NC FBC CMD29  |  |
| FBC_CMD30   | A20 | NC FBC CMD30  |  |
| FBC_CLK0    | E17 | FB B CLK P<0> |  |
| FBC_CLK0*   | D17 | FB B CLK N<0> |  |
| FBC_CLK1    | D23 | FB B CLK P<1> |  |
| FBC_CLK1*   | E23 | FB B CLK N<1> |  |
| FBC_DQM0    | F11 | FB B DQM L<0> |  |
| FBC_DQM1    | D10 | FB B DQM L<1> |  |
| FBC_DQM2    | D15 | FB B DQM L<2> |  |
| FBC_DQM3    | A16 | FB B DQM L<3> |  |
| FBC_DQM4    | D27 | FB B DQM L<4> |  |
| FBC_DQM5    | D28 | FB B DQM L<5> |  |
| FBC_DQM6    | D34 | FB B DQM L<6> |  |
| FBC_DQM7    | A34 | FB B DQM L<7> |  |
| FBC_DQS_RN0 | D9  | FB B RDQS<0>  |  |
| FBC_DQS_RN1 | B10 | FB B RDQS<1>  |  |
| FBC_DQS_RN2 | E14 | FB B RDQS<2>  |  |
| FBC_DQS_RN3 | B14 | FB B RDQS<3>  |  |
| FBC_DQS_RN4 | F26 | FB B RDQS<4>  |  |
| FBC_DQS_RN5 | A26 | FB B RDQS<5>  |  |
| FBC_DQS_RN6 | D31 | FB B RDQS<6>  |  |
| FBC_DQS_RN7 | A31 | FB B RDQS<7>  |  |
| FBC_DQS_WP0 | E10 | FB B WDQS<0>  |  |
| FBC_DQS_WP1 | A10 | FB B WDQS<1>  |  |
| FBC_DQS_WP2 | D14 | FB B WDQS<2>  |  |
| FBC_DQS_WP3 | C14 | FB B WDQS<3>  |  |
| FBC_DQS_WP4 | E26 | FB B WDQS<4>  |  |
| FBC_DQS_WP5 | B26 | FB B WDQS<5>  |  |
| FBC_DQS_WP6 | D32 | FB B WDQS<6>  |  |
| FBC_DQS_WP7 | A32 | FB B WDQS<7>  |  |
| FB_DLLAVDD1 | J19 |               |  |
| FB_PLLAVDD1 | J18 |               |  |
| FBC_DEBUG   | G19 | FBC DEBUG     |  |
| FB_VREF     | J27 |               |  |
| FBC_RFU0    | G11 |               |  |
| FBC_RFU1*   | G12 |               |  |
| FBC_RFU2    | G14 |               |  |
| FBC_RFU3*   | G15 |               |  |
| FBC_RFU4    | G16 |               |  |
| FBC_RFU5*   | G17 |               |  |
| FBC_RFU6    | G18 |               |  |
| FBC_RFU7*   | G19 |               |  |



NV G96 Frame Buffer I/F

SYNC\_MASTER=MUXGF SYNC\_DATE=07/10/2008

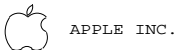
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APPLE INC.

SIZE D DRAWING NUMBER 051-7892 REV. A.0.0

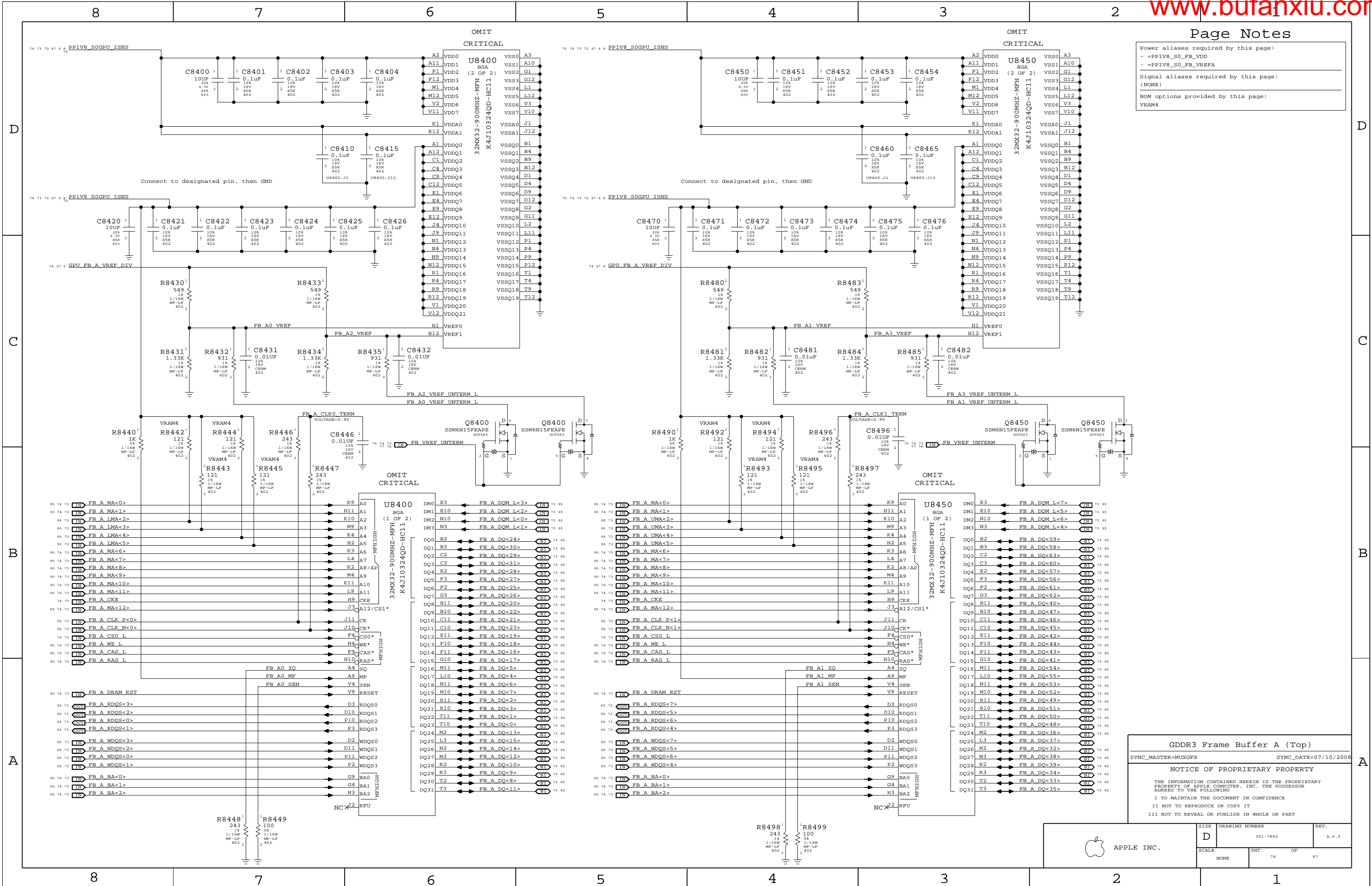
SCALE NONE SHT 73 OF 97



Power aliases required by this page:  
- =PPIV8\_S0\_FB\_VDD  
- =PPIV8\_S0\_FB\_VREFA

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
VRAM4



GDDR3 Frame Buffer A (Top)

SYNC\_MASTER=MUXGFX SYNC\_DATE=07/10/2008

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| SIZE  | DRAWING NUMBER | REV.  |
|-------|----------------|-------|
| D     | 051-7892       | A.0.0 |
| SCALE | SIT            | OF    |
| NONE  | 74             | 97    |





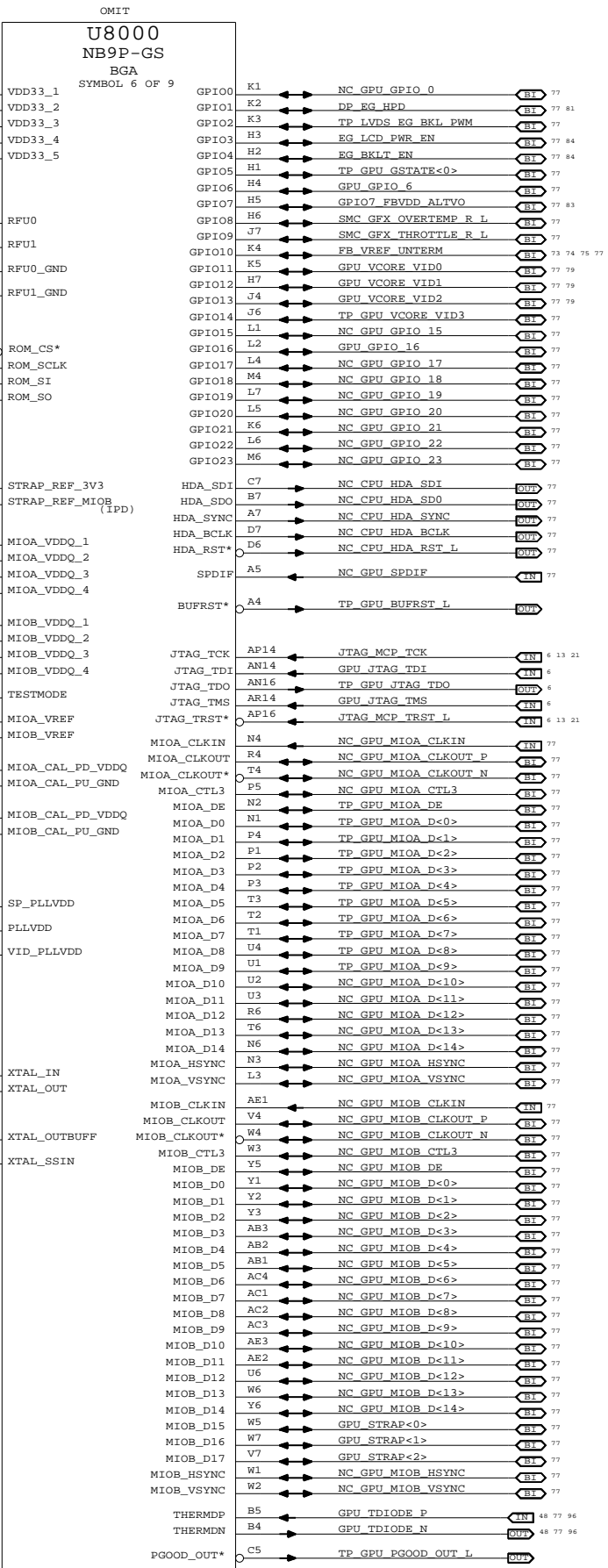
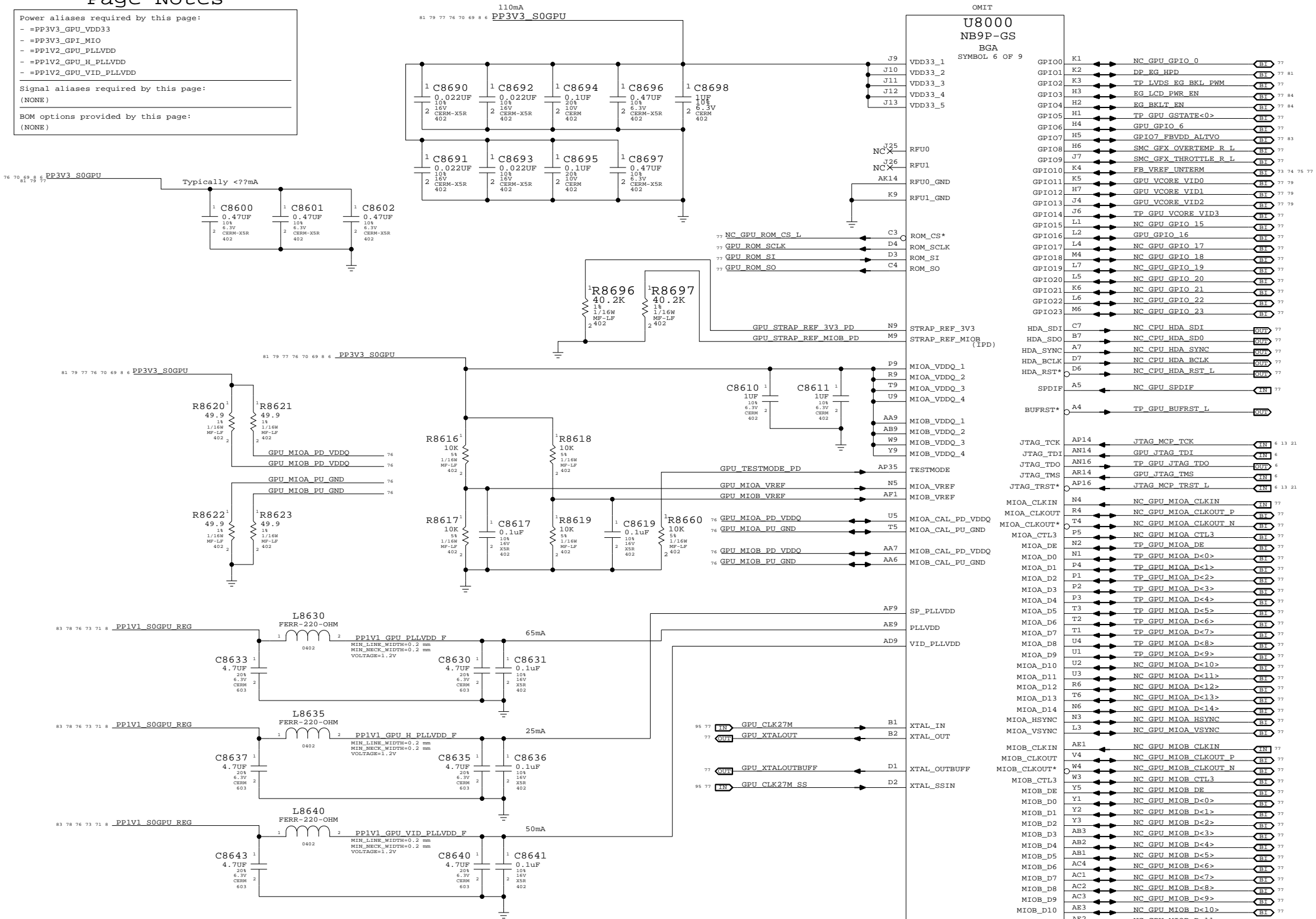


Page Notes

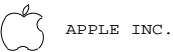
Power aliases required by this page:  
- =PP3V3\_GPU\_VDD33  
- =PP3V3\_GPU\_MIO  
- =PP1V2\_GPU\_PLLVDD  
- =PP1V2\_GPU\_H\_PLLVDD  
- =PP1V2\_GPU\_VID\_PLLVDD

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)



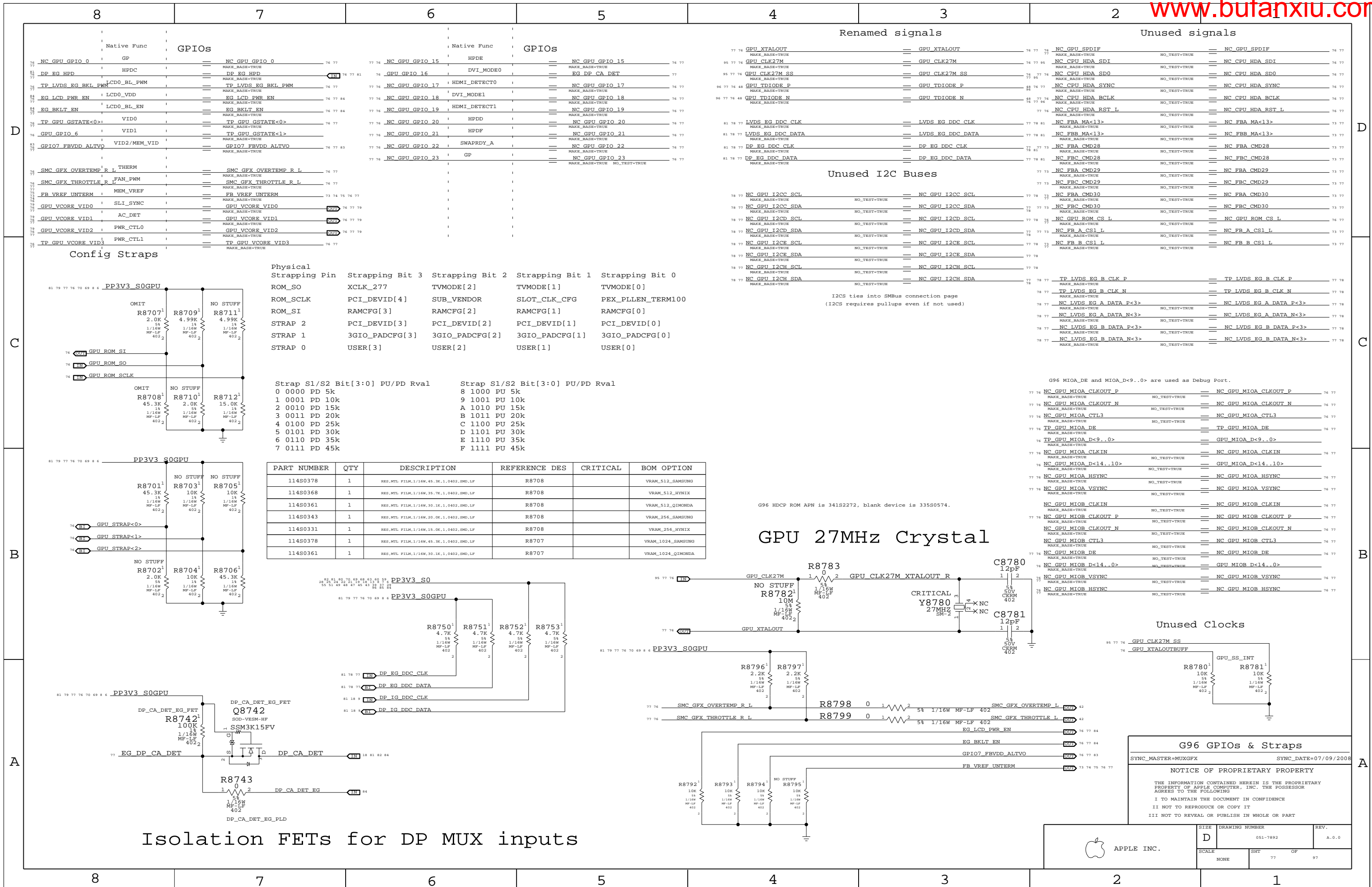
| NV G96 GPIO/MIO/Misc                                                                                                       |                      |
|----------------------------------------------------------------------------------------------------------------------------|----------------------|
| SYNC_MASTER=MUXGFX                                                                                                         | SYNC_DATE=07/10/2008 |
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APPLE INC.

| SIZE  | DRAWING NUMBER | REV.  |
|-------|----------------|-------|
| D     | 051-7892       | A.0.0 |
| SCALE | SHT            | OF    |
| NONE  | 76             | 97    |







Power aliases required by this page:

- =PP1V8\_GPU\_IPFX
- =PP3V3\_GPU\_IPFXD\_IOVDD

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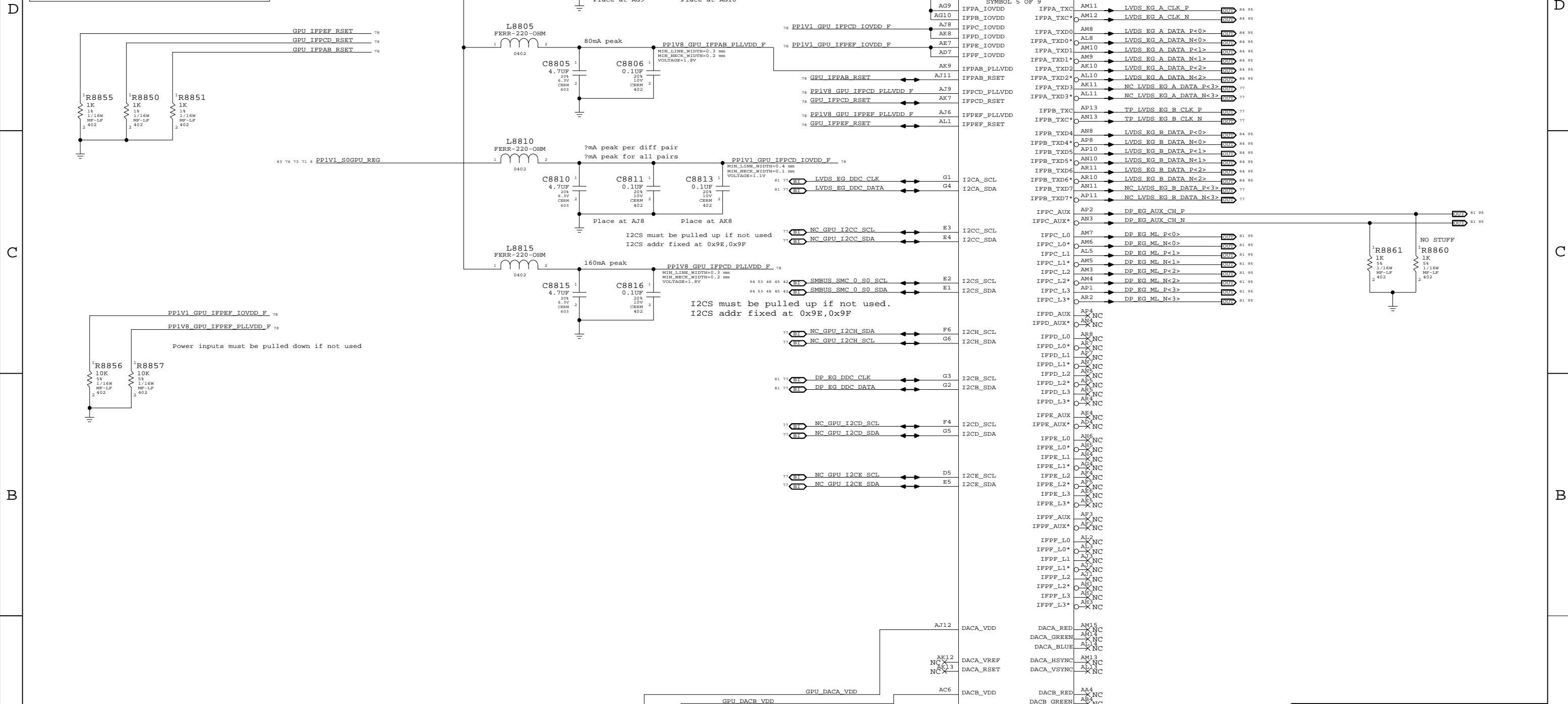
Signal aliases required by this page:

(NONE)

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BOM options provided by this page:

(NONE)

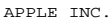


SYNC\_MASTER=MUXGFX SYNC\_DATE=07/10/2008

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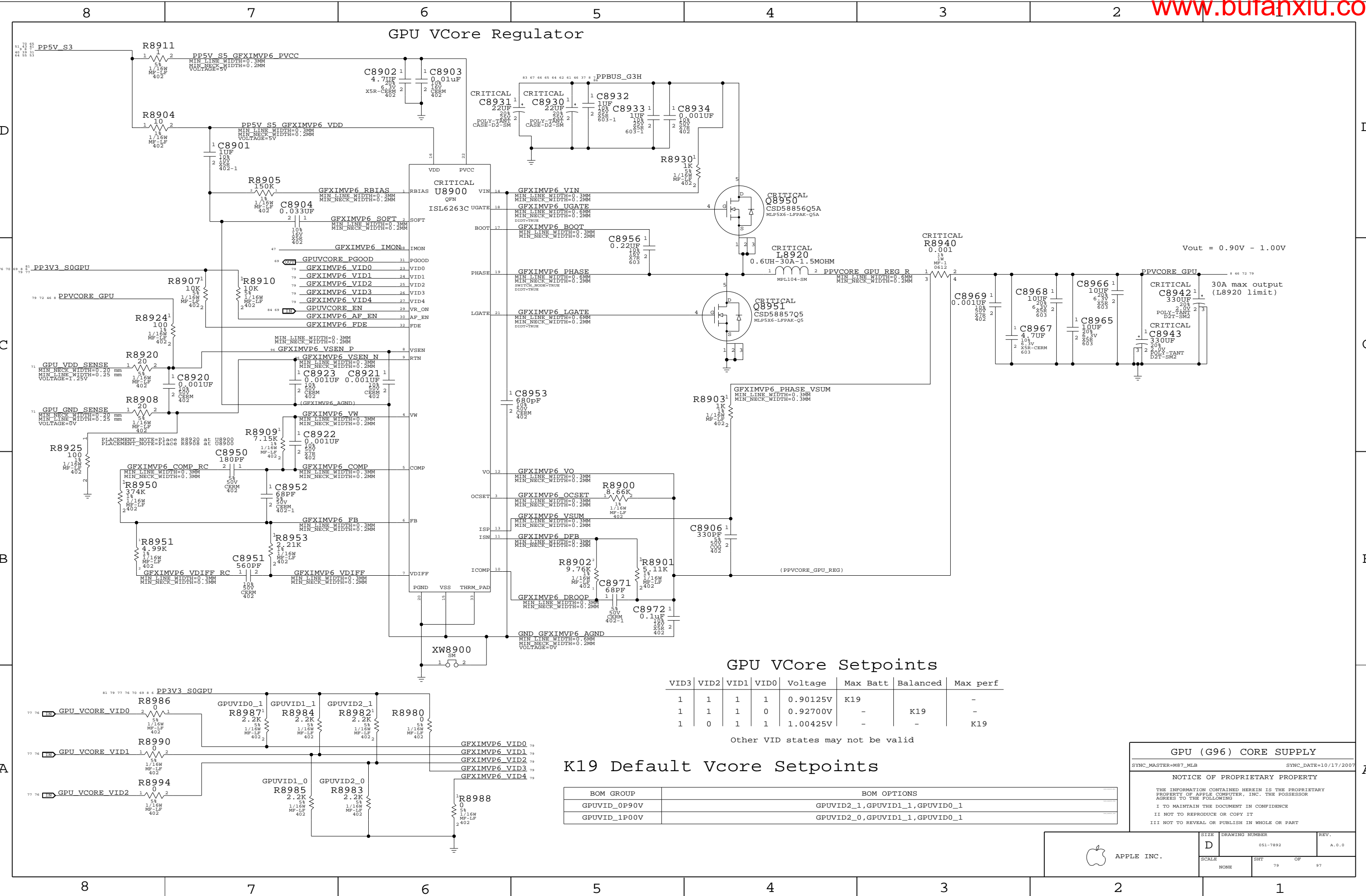
II NOT TO REPRODUCE OR COPY IT



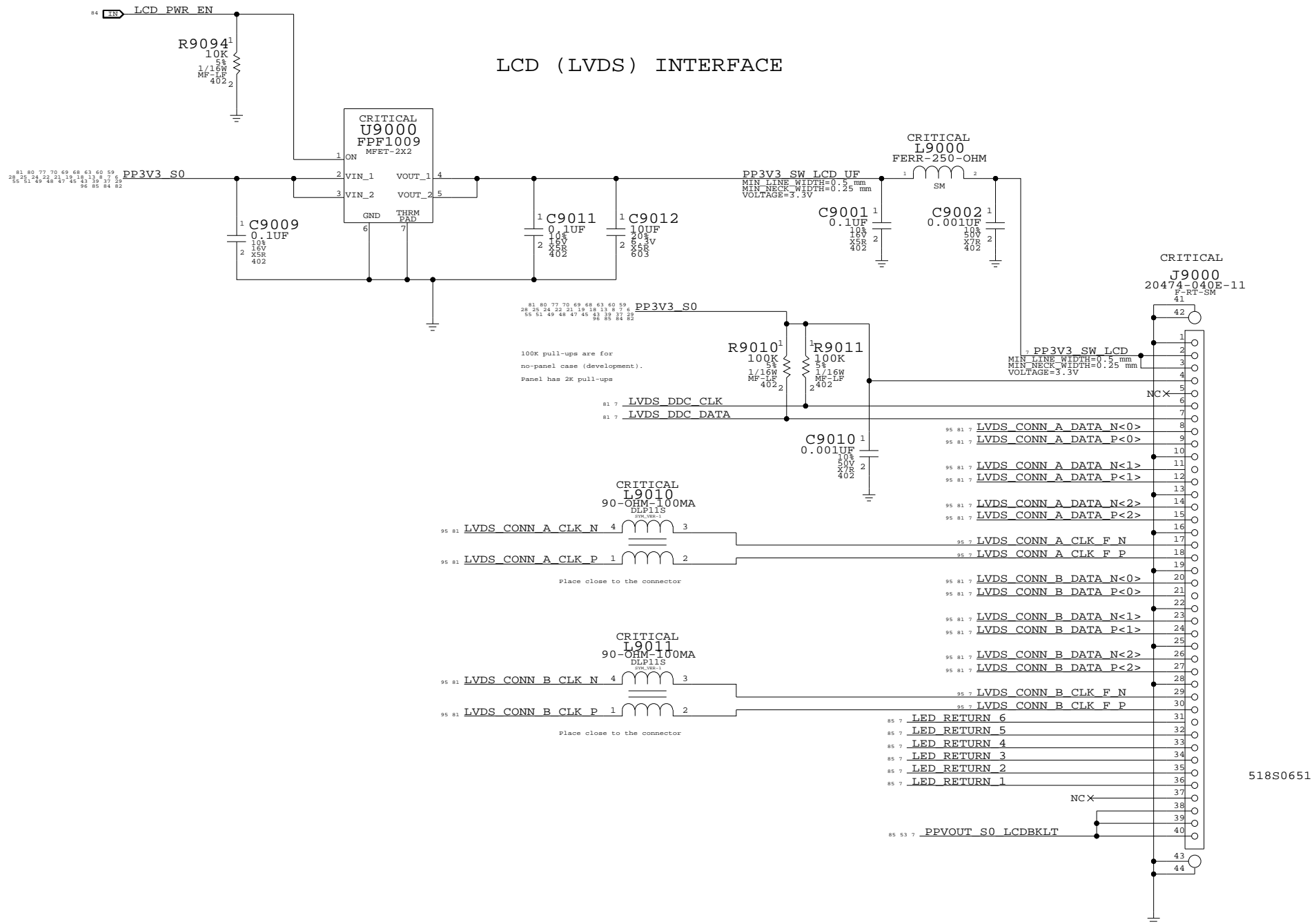
|   |          |      |
|---|----------|------|
| D | 051-7892 | A.O. |
|---|----------|------|

|      |  |
|------|--|
| NONE |  |
|------|--|









LVDS Display Connector

SYNC\_MASTER=D0R SYNC\_DATE=12/19/2008

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## D

C

B

A

|   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|
| 8 | 7 | 6 | 5 | 4 | 3 | 2 |
|---|---|---|---|---|---|---|

[illegible]

D

C

B

A

70, 69, 68, 63, 60, 59  
19, 18, 13, 8, 7, 6  
47, 45, 43, 39, 37, 35  
32, 25, 24

PP3V3 S0

C9370  
0.1µF  
20V  
CERM  
402

U9370  
SN74LV4066A

R9370<sup>1</sup>  
20K  
1/16W  
MF-LF  
402 2

R9371<sup>1</sup>  
20K  
1/16W  
MF-LF  
402 2

R9372<sup>1</sup>  
20K  
1/16W  
MF-LF  
402 2

R9373<sup>1</sup>  
20K  
1/16W  
MF-LF  
402 2

LVDS DDC SEL EG

LVDS DDC SEL IG

LVDS EG DDC CLK

LVDS IG DDC CLK

LVDS DDC CLK

LVDS EG DDC DATA

LVDS IG DDC DATA

LVDS DDC DATA

77 78

18

7 80

77 78

18

7 80

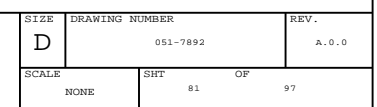
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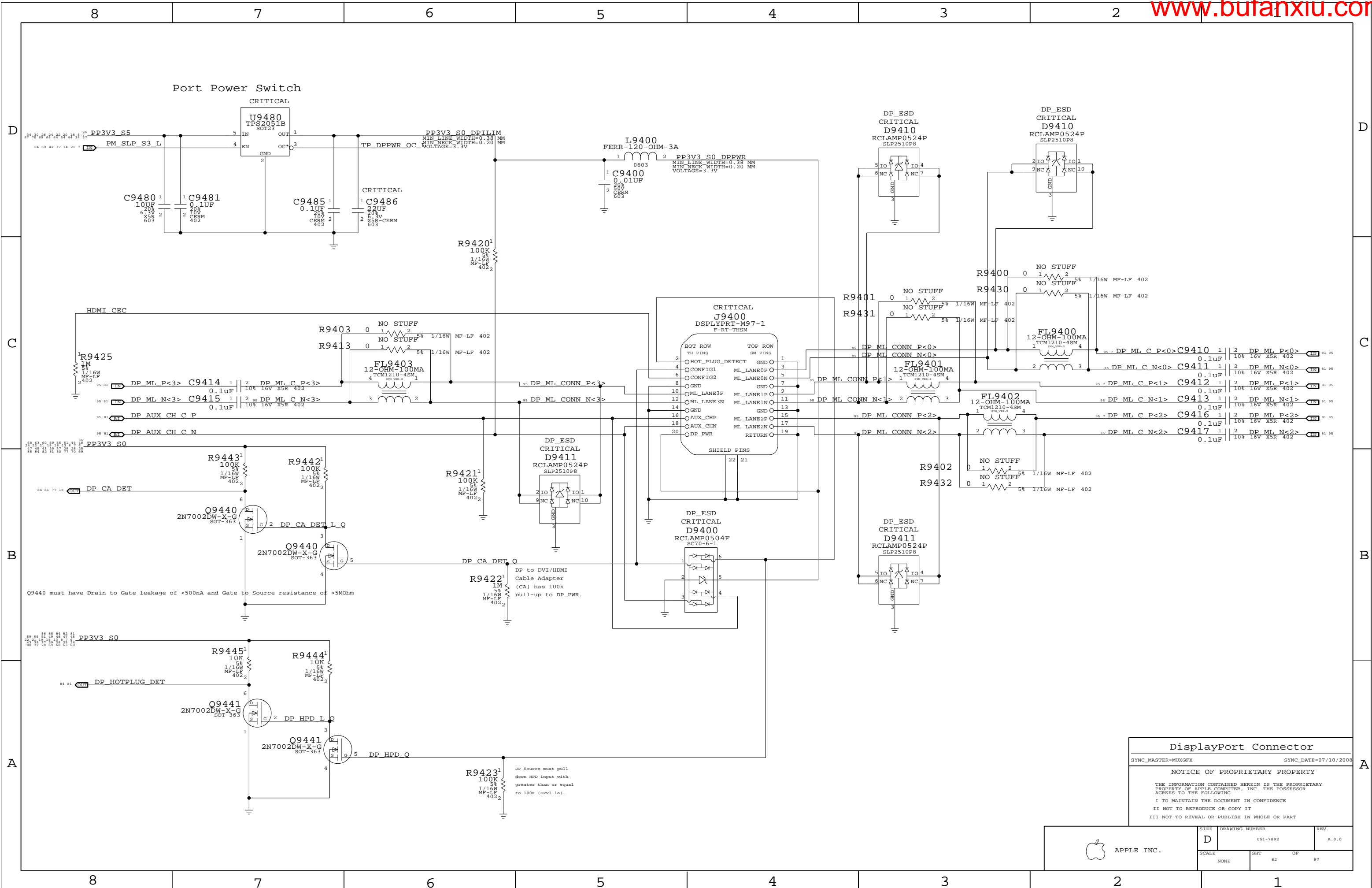
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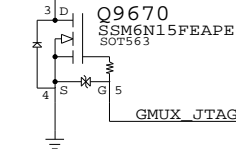





BA

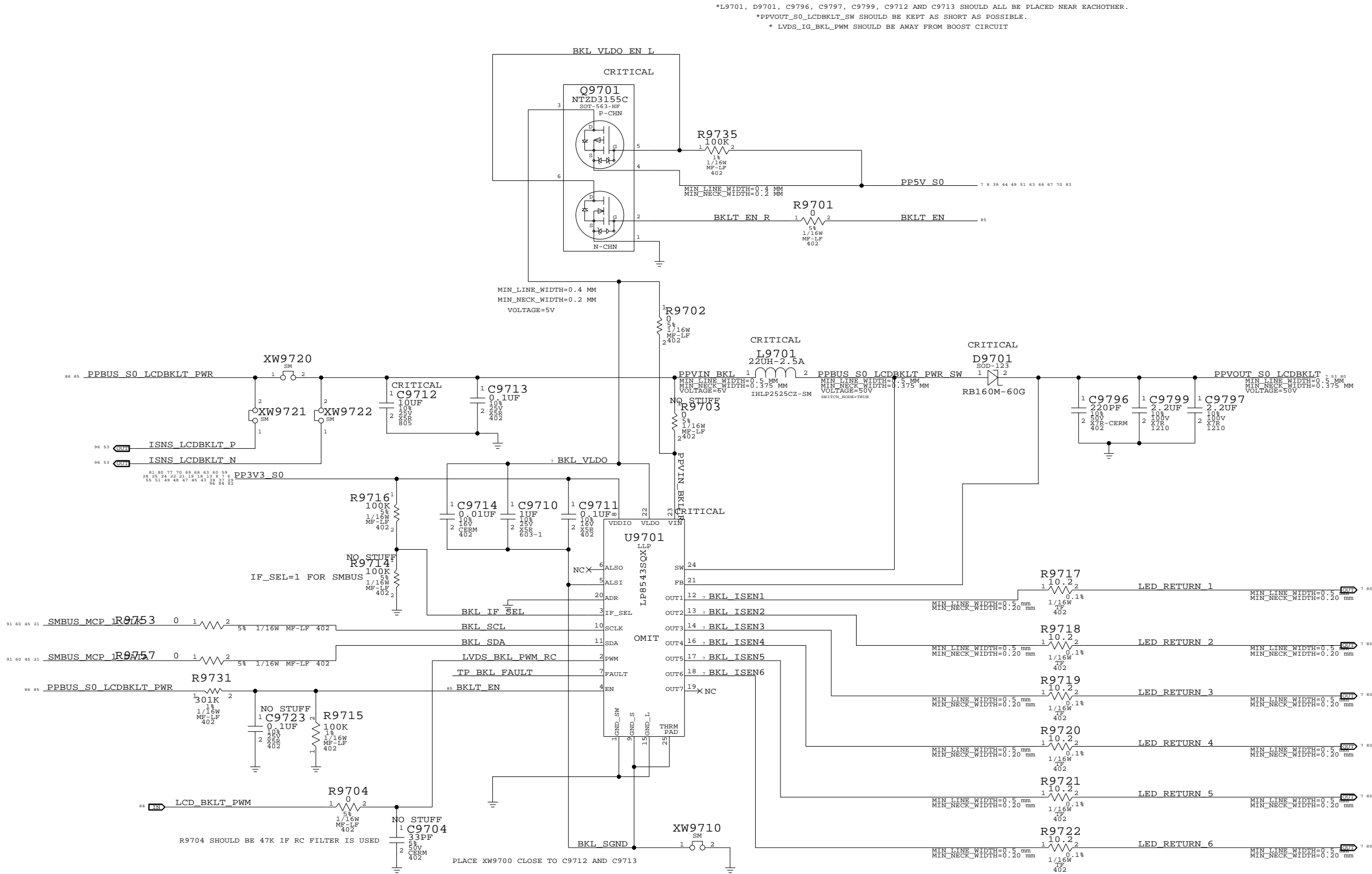


GMUX\_JTAG\_TCK Inversion



|                                                                                                  |       |                |       |
|--------------------------------------------------------------------------------------------------|-------|----------------|-------|
|  APPLE INC. | SIZE  | DRAWING NUMBER | REV.  |
|                                                                                                  | D     | 051-7892       | A.0.0 |
|                                                                                                  | SCALE | SHT            | OF    |
|                                                                                                  | NONE  | 84             | 97    |





| PART#    | QTY | DESCRIPTION                 | REFERENCE DESIGNATOR(S) | CRITICAL | BOM OPTION |
|----------|-----|-----------------------------|-------------------------|----------|------------|
| 353S2670 | 1   | IC,LP8543,WHT LED BKLT,PROD | U9701                   | CRITICAL |            |

LCD BACKLIGHT DRIVER

SYNC\_MASTER=DDR

SYNC\_DATE=12/12/2008

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APPLE INC.

SCALE  
NONE

SIZE  
D

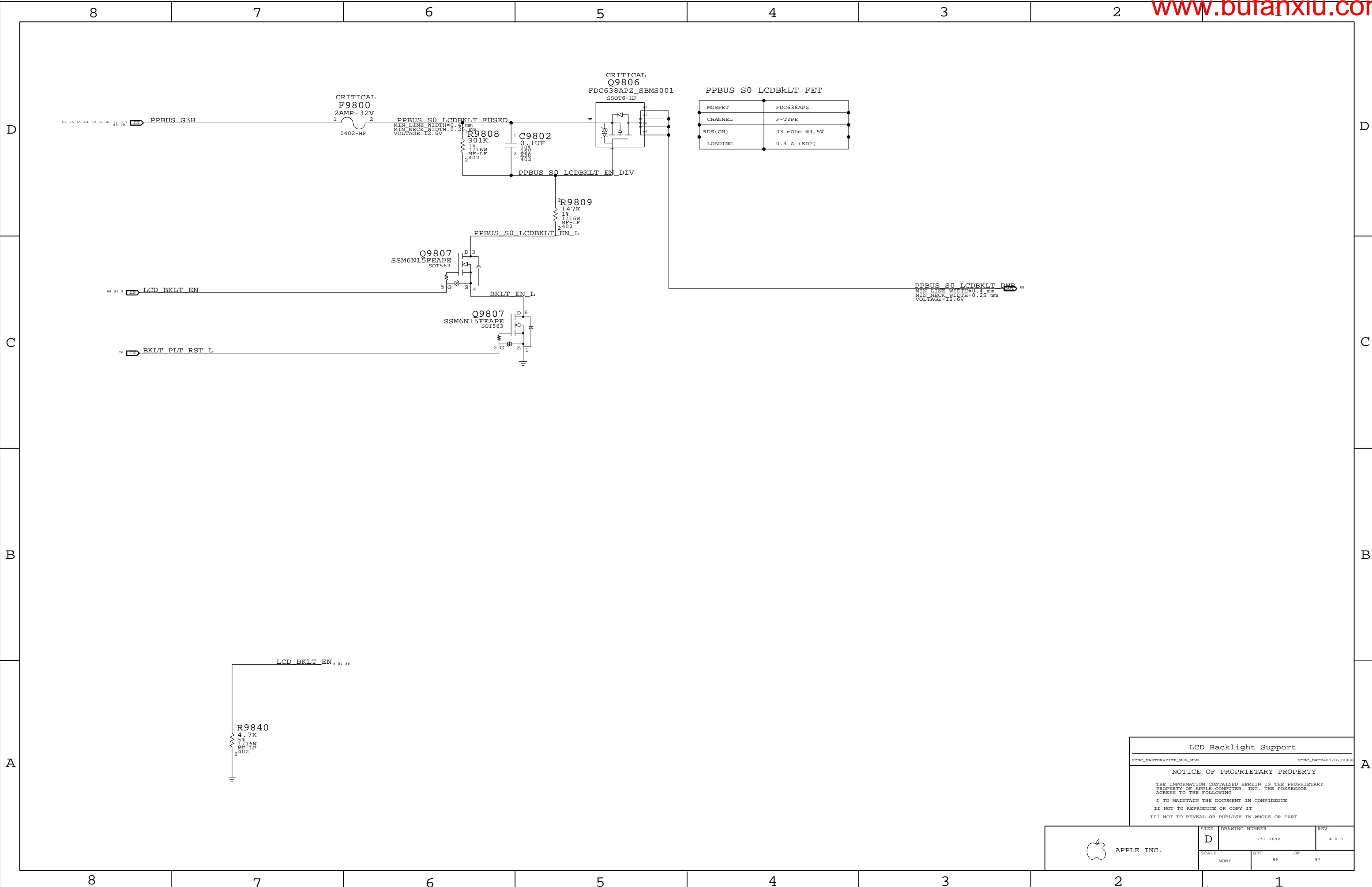
DRAWING NUMBER  
051-7892

SHT  
85

REV.  
A.0.0

OF  
97





LCD Backlight Support

SYNC\_MASTER=VITE\_M98\_MLS

SYNC\_DATE=07/02/2008

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SIZE D

DRAWING NUMBER 051-7892

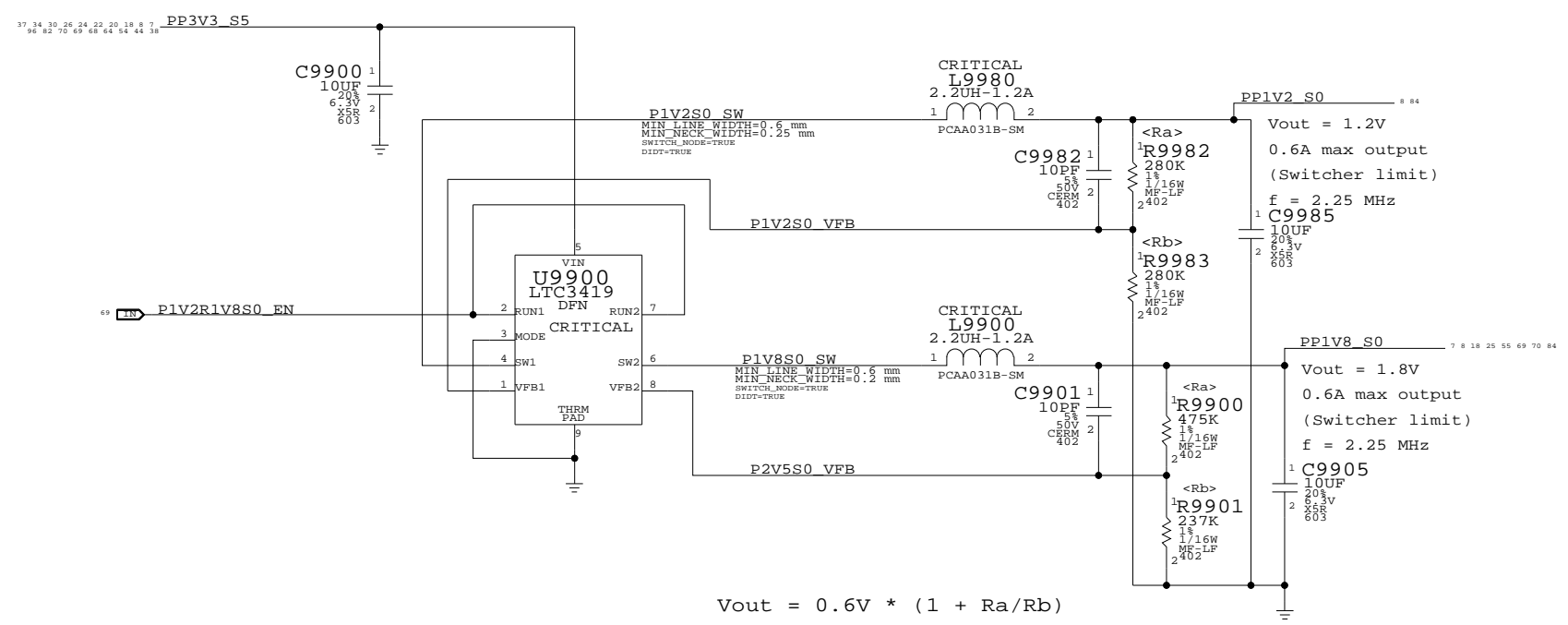
REV. A.0.0

SCALE NONE

SHT 86 OF 97



1.8V/1.2V S0 SWITCHER



Misc Power Supplies

SYNC\_MASTER=MUXGFX SYNC\_DATE=02/01/2008

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|            |      |                |       |
|------------|------|----------------|-------|
| APPLE INC. | SIZE | DRAWING NUMBER | REV.  |
|            | D    | 051-7892       | A.0.0 |
| SCALE      |      | SHT            | OF    |
| NONE       |      | 87             | 97    |



FSB (Front-Side Bus) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| FSB_50S           | *     | =50_OHM_SE            | =50_OHM_SE         | =50_OHM_SE         | =50_OHM_SE          | =STANDARD            | =STANDARD         |
| FSB_DSTB_50S      | *     | =50_OHM_SE            | =50_OHM_SE         | =50_OHM_SE         | =50_OHM_SE          | =1:1_DIFFPAIR        | =1:1_DIFFPAIR     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| FSB_DATA         | *     | =2x_DIELECTRIC       | ?      | FSB_DATA         | TOP,BOTTOM | =4x_DIELECTRIC       | ?      |
| FSB_DSTB         | *     | =3x_DIELECTRIC       | ?      | FSB_DSTB         | TOP,BOTTOM | =5x_DIELECTRIC       | ?      |
| FSB_ADDR         | *     | =STANDARD            | ?      | FSB_ADDR         | TOP,BOTTOM | =3x_DIELECTRIC       | ?      |
| FSB_ADSTB        | *     | =2x_DIELECTRIC       | ?      | FSB_ADSTB        | TOP,BOTTOM | =4x_DIELECTRIC       | ?      |
| FSB_1X           | *     | =STANDARD            | ?      | FSB_1X           | TOP,BOTTOM | =3x_DIELECTRIC       | ?      |

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.  
Signals within each 4x group should be matched within 5 ps of strobe.  
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.  
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.  
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.  
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.  
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.  
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.  
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CPU_50S           | *     | =50_OHM_SE            | =50_OHM_SE         | =50_OHM_SE         | =50_OHM_SE          | =STANDARD            | =STANDARD         |
| CPU_27P4S         | *     | =27P4_OHM_SE          | =27P4_OHM_SE       | =27P4_OHM_SE       | =27P4_OHM_SE        | 7 MIL                | 7 MIL             |

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| CPU_AGTL         | *     | =STANDARD            | ?      | CPU_AGTL         | TOP,BOTTOM | =2x_DIELECTRIC       | ?      |
| CPU_8MIL         | *     | 8 MIL                | ?      |                  |            |                      |        |
| CPU_COMP         | *     | 25 MIL               | ?      |                  |            |                      |        |
| CPU_GTLREF       | *     | 25 MIL               | ?      |                  |            |                      |        |
| CPU_ITP          | *     | =2:1_SPACING         | ?      |                  |            |                      |        |
| CPU_VCCSENSE     | *     | 25 MIL               | ?      |                  |            |                      |        |

Most CPU signals with impedance requirements are 55-ohm single-ended.  
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MCP_50S           | *     | =50_OHM_SE            | =50_OHM_SE         | =50_OHM_SE         | =50_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| MCP_FSB_COMP     | *     | 8 MIL                | ?      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.4

FSB Clock Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CLK_FSB_100D      | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| CLK_FSB          | *     | =3x_DIELECTRIC       | ?      | CLK_FSB          | TOP,BOTTOM | =4x_DIELECTRIC       | ?      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v01), Section 2.2.5

CPU / FSB Net Properties

|                      | ELECTRICAL_CONSTRAINT_SET | NET_TYPE     |              |                           |
|----------------------|---------------------------|--------------|--------------|---------------------------|
|                      |                           | PHYSICAL     | SPACING      |                           |
| FSB 4X Signal Groups | FSB_DATA_GROUP0           | FSB_50S      | FSB_DATA     | FSB D L<15..0> 7 10 14    |
|                      | FSB_DATA_GROUP0           | FSB_50S      | FSB_DATA     | FSB DINV L<0> 7 10 14     |
|                      | FSB_DSTB0                 | FSB_DSTB_50S | FSB_DSTB     | FSB DSTB L P<0> 7 10 14   |
|                      | FSB_DSTB0                 | FSB_DSTB_50S | FSB_DSTB     | FSB DSTB L N<0> 7 10 14   |
|                      | FSB_DATA_GROUP1           | FSB_50S      | FSB_DATA     | FSB D L<31..16> 7 10 14   |
|                      | FSB_DATA_GROUP1           | FSB_50S      | FSB_DATA     | FSB DINV L<1> 7 10 14     |
|                      | FSB_DSTR1                 | FSB_DSTR_50S | FSB_DSTR     | FSB DSTB L P<1> 7 10 14   |
|                      | FSB_DSTB1                 | FSB_DSTB_50S | FSB_DSTB     | FSB DSTB L N<1> 7 10 14   |
|                      | FSB_DATA_GROUP2           | FSB_50S      | FSB_DATA     | FSB D L<47..32> 7 10 14   |
|                      | FSB_DATA_GROUP2           | FSB_50S      | FSB_DATA     | FSB DINV L<2> 7 10 14     |
|                      | FSB_DSTB2                 | FSB_DSTB_50S | FSB_DSTB     | FSB DSTB L P<2> 7 10 14   |
|                      | FSB_DSTB2                 | FSB_DSTB_50S | FSB_DSTB     | FSB DSTB L N<2> 7 10 14   |
| FSB 2X Signals       | FSB_DATA_GROUP3           | FSB_50S      | FSB_DATA     | FSB D L<63..48> 7 10 14   |
|                      | FSB_DATA_GROUP3           | FSB_50S      | FSB_DATA     | FSB DINV L<3> 7 10 14     |
|                      | FSB_DSTR3                 | FSB_DSTR_50S | FSB_DSTR     | FSB DSTB L P<3> 7 10 14   |
|                      | FSB_DSTR3                 | FSB_DSTR_50S | FSB_DSTR     | FSB DSTB L N<3> 7 10 14   |
|                      | FSB_ADDR_GROUP0           | FSB_50S      | FSB_ADDR     | FSB A L<16..3> 7 10 14    |
|                      | FSB_ADDR_GROUP0           | FSB_50S      | FSB_ADDR     | FSB REQ L<4..0> 10 14     |
|                      | FSB_ADSTR0                | FSB_50S      | FSB_ADSTR    | FSB ADSTB L<0> 7 10 14    |
|                      | FSB_ADDR_GROUP1           | FSB_50S      | FSB_ADDR     | FSB A L<35..17> 7 10 14   |
|                      | FSB_ADSTR1                | FSB_50S      | FSB_ADSTR    | FSB ADSTB L<1> 7 10 14    |
|                      | FSB_1X                    | FSB_50S      | FSB_1X       | FSB ADS L 7 10 14         |
|                      | FSB_BREQ0_L               | FSB_50S      | FSB_1X       | FSB_BREQ0 L 9 10 14       |
|                      | FSB_BREQ1_L               | FSB_50S      | FSB_1X       | FSB_BREQ1 L 14            |
| FSB 1X Signals       | FSB_1X                    | FSB_50S      | FSB_1X       | FSB BNR L 10 14           |
|                      | FSB_1X                    | FSB_50S      | FSB_1X       | FSB BPRI L 10 14          |
|                      | FSB_1X                    | FSB_50S      | FSB_1X       | FSB DBSY L 10 14          |
|                      | FSB_1X                    | FSB_50S      | FSB_1X       | FSB DEFER L 10 14         |
|                      | FSB_1X                    | FSB_50S      | FSB_1X       | FSB DRDY L 10 14          |
|                      | FSB_1X                    | FSB_50S      | FSB_1X       | FSB HIT L 7 10 14         |
|                      | FSB_1X                    | FSB_50S      | FSB_1X       | FSB HITM L 7 10 14        |
|                      | FSB_1X                    | FSB_50S      | FSB_1X       | FSB LOCK L 7 10 14        |
|                      | FSB_CPURST_L              | FSB_50S      | FSB_1X       | FSB CPURST L 9 10 13 14   |
|                      | FSB_1X                    | FSB_50S      | FSB_1X       | FSB RS L<2..0> 10 14      |
|                      | FSB_1X                    | FSB_50S      | FSB_1X       | FSB TRDY L 10 14          |
|                      | CPU_ASYNC                 | CPU_50S      | CPU_AGTL     | CPU A20M L 10 14          |
| FSB 1X Signals       | CPU_BSEL                  | CPU_50S      | CPU_AGTL     | CPU BSEL<2..0> 9 10       |
|                      | CPU_FERR_L                | CPU_50S      | CPU_8MIL     | CPU FERR L 10 14          |
|                      | CPU_ASYNC                 | CPU_50S      | CPU_AGTL     | CPU IGNNE L 10 14         |
|                      | CPU_INIT_L                | CPU_50S      | CPU_AGTL     | CPU INIT L 10 14          |
|                      | CPU_ASYNC_R               | CPU_50S      | CPU_AGTL     | CPU INTR 9 10 14          |
|                      | CPU_ASYNC_R               | CPU_50S      | CPU_AGTL     | CPU NMI 9 10 14           |
|                      | CPU_PROCHOT_L             | CPU_50S      | CPU_AGTL     | CPU PROCHOT L 10 14 43 63 |
|                      | CPU_PWRGD                 | CPU_50S      | CPU_AGTL     | CPU PWRGD 10 13 14        |
|                      | CPU_ASYNC                 | CPU_50S      | CPU_AGTL     | CPU SMI L 10 14           |
|                      | CPU_ASYNC                 | CPU_50S      | CPU_AGTL     | CPU STPCLK L 10 14        |
|                      | PM_THRMTRIP_L             | CPU_50S      | CPU_8MIL     | PM THRMTRIP L 10 14 43    |
|                      | FSB_CPUSLP_L              | CPU_50S      | CPU_AGTL     | FSB CPUSLP L 10 14        |
| FSB 1X Signals       | CPU_FROM_SR               | CPU_50S      | CPU_AGTL     | CPU DPSLP L 10 14         |
|                      | CPU DPRSTP_L              | CPU_50S      | CPU_AGTL     | CPU DPRSTP L 9 10 14 63   |
|                      | CPU_ASYNC                 | CPU_50S      | CPU_AGTL     | FSB DPWR L 10 14          |
|                      | MCP_CPU_COMP              | MCP_50S      | MCP_FSB_COMP | MCP BCLK VML COMP VDD 14  |
|                      | MCP_CPU_COMP              | MCP_50S      | MCP_FSB_COMP | MCP BCLK VML COMP GND 14  |
|                      | MCP_CPU_COMP              | MCP_50S      | MCP_FSB_COMP | MCP CPU COMP VCC 14       |
|                      | MCP_CPU_COMP              | MCP_50S      | MCP_FSB_COMP | MCP CPU COMP GND 14       |
|                      | FSB_CLK_CPU               | CLK_FSB_100D | CLK_FSB      | FSB CLK CPU P 10 14       |
|                      | FSB_CLK_CPU               | CLK_FSB_100D | CLK_FSB      | FSB CLK CPU N 10 14       |
|                      | FSB_CLK_ITP               | CLK_FSB_100D | CLK_FSB      | FSB CLK ITP P 13 14       |
|                      | FSB_CLK_ITP               | CLK_FSB_100D | CLK_FSB      | FSB CLK ITP N 13 14       |
|                      | FSB_CLK_MCP               | CLK_FSB_100D | CLK_FSB      | FSB CLK MCP P 14          |
|                      | FSB_CLK_MCP               | CLK_FSB_100D | CLK_FSB      | FSB CLK MCP N 14          |
| FSB 1X Signals       | CPU_IERR_L                | CPU_50S      |              | CPU IERR L 10             |
|                      | PM DPRSLPVR               | CPU_50S      | CPU_AGTL     | PM DPRSLPVR 21 63         |
|                      | (See above)               | CPU_50S      | CPU_AGTL     | IMVP DPRSLPVR 63          |
|                      | CPU_GTLREF                | CPU_50S      | CPU_GTLREF   | CPU GTLREF 10 27          |
|                      | CPU_COMP                  | CPU_50S      | CPU_COMP     | CPU COMP<3> 10            |
|                      | CPU_COMP                  | CPU_27P4S    | CPU_COMP     | CPU COMP<2> 10            |
|                      | CPU_COMP                  | CPU_50S      | CPU_COMP     | CPU COMP<1> 10            |
|                      | CPU_COMP                  | CPU_27P4S    | CPU_COMP     | CPU COMP<0> 10            |
|                      | XDP_TDI                   | CPU_50S      | CPU_ITP      | XDP TDI 6 10 13           |
|                      | XDP_TDO                   | CPU_50S      | CPU_ITP      | XDP TDO 6 10              |
|                      | XDP_TMS                   | CPU_50S      | CPU_ITP      | XDP TMS 6 10 13           |
|                      | XDP_TCK                   | CPU_50S      | CPU_ITP      | XDP TCK 6 10 13           |
| FSB 1X Signals       | XDP_TRST_L                | CPU_50S      | CPU_ITP      | XDP TRST L 6 10 13        |
|                      | XDP_BPM_L                 | CPU_50S      | CPU_ITP      | XDP BPM L<4..0> 10 13     |
|                      | XDP_BPM_L5                | CPU_50S      | CPU_ITP      | XDP BPM L<5> 10 13        |
|                      | (FSB_CPURST_L)            | CPU_50S      | CPU_ITP      | XDP CPURST L 13           |
|                      |                           | CPU_50S      | CPU_8MIL     | CPU VID<6..0> 9 11        |
|                      |                           | CPU_50S      | CPU_8MIL     | IMVP6 VID<6..0> 9 63      |
|                      | CPU_VCCSENSE              | CPU_27P4S    | CPU_VCCSENSE | CPU VCCSENSE_P 11 63      |
|                      | CPU_VCCSENSE              | CPU_27P4S    | CPU_VCCSENSE | CPU VCCSENSE_N 11 63      |
|                      | (CPU_VCCSENSE)            | CPU_27P4S    | CPU_VCCSENSE | IMVP6 VSEN_P 63           |
|                      | (CPU_VCCSENSE)            | CPU_27P4S    | CPU_VCCSENSE | IMVP6 VSEN_N 63           |

CPU/FSB Constraints

SYNC\_MASTER=MUXGFX SYNC\_DATE=02/18/2008

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Memory Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MEM_40S           | *     | =40_OHM_SE            | =40_OHM_SE         | =40_OHM_SE         | =40_OHM_SE          | =STANDARD            | =STANDARD         |
| MEM_40S_VDD       | *     | =40_OHM_SE            | =40_OHM_SE         | =40_OHM_SE         | =40_OHM_SE          | =STANDARD            | =STANDARD         |
| MEM_70D           | *     | =70_OHM_DIFF          | =70_OHM_DIFF       | =70_OHM_DIFF       | =70_OHM_DIFF        | =70_OHM_DIFF         | =70_OHM_DIFF      |
| MEM_70D_VDD       | *     | =70_OHM_DIFF          | =70_OHM_DIFF       | =70_OHM_DIFF       | =70_OHM_DIFF        | =70_OHM_DIFF         | =70_OHM_DIFF      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| MEM_CLK2MEM      | *     | =4:1_SPACING         | ?      |
| MEM_CTRL2CTRL    | *     | =2:1_SPACING         | ?      |
| MEM_CTRL2MEM     | *     | =2.5:1_SPACING       | ?      |
| MEM_CMD2CMD      | *     | =1.5:1_SPACING       | ?      |
| MEM_CMD2MEM      | *     | =3:1_SPACING         | ?      |
| MEM_DATA2DATA    | *     | =1.5:1_SPACING       | ?      |
| MEM_DATA2MEM     | *     | =3:1_SPACING         | ?      |
| MEM_DQS2MEM      | *     | =3:1_SPACING         | ?      |
| MEM_2OTHER       | *     | 25 MIL               | ?      |

Memory Bus Spacing Group Assignments

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CLK           | MEM_CLK           | *         | MEM_CLK2MEM      |
| MEM_CLK           | MEM_CTRL          | *         | MEM_CLK2MEM      |
| MEM_CLK           | MEM_CMD           | *         | MEM_CLK2MEM      |
| MEM_CLK           | MEM_DATA          | *         | MEM_CLK2MEM      |
| MEM_CLK           | MEM_DQS           | *         | MEM_CLK2MEM      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CMD           | MEM_CLK           | *         | MEM_CMD2MEM      |
| MEM_CMD           | MEM_CTRL          | *         | MEM_CMD2MEM      |
| MEM_CMD           | MEM_CMD           | *         | MEM_CMD2CMD      |
| MEM_CMD           | MEM_DATA          | *         | MEM_CMD2MEM      |
| MEM_CMD           | MEM_DQS           | *         | MEM_CMD2MEM      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CTRL          | MEM_CLK           | *         | MEM_CTRL2MEM     |
| MEM_CTRL          | MEM_CTRL          | *         | MEM_CTRL2CTRL    |
| MEM_CTRL          | MEM_CMD           | *         | MEM_CTRL2MEM     |
| MEM_CTRL          | MEM_DATA          | *         | MEM_CTRL2MEM     |
| MEM_CTRL          | MEM_DQS           | *         | MEM_CTRL2MEM     |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_DQS           | MEM_CLK           | *         | MEM_DQS2MEM      |
| MEM_DQS           | MEM_CTRL          | *         | MEM_DQS2MEM      |
| MEM_DQS           | MEM_CMD           | *         | MEM_DQS2MEM      |
| MEM_DQS           | MEM_DATA          | *         | MEM_DQS2MEM      |
| MEM_DQS           | MEM_DQS           | *         | MEM_DQS2MEM      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CLK           | *                 | *         | MEM_2OTHER       |
| MEM_CTRL          | *                 | *         | MEM_2OTHER       |
| MEM_CMD           | *                 | *         | MEM_2OTHER       |
| MEM_DATA          | *                 | *         | MEM_2OTHER       |
| MEM_DQS           | *                 | *         | MEM_2OTHER       |

Need to support MEM\_\*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.

All DQS pairs should be matched within 100 ps of clocks.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.

A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps

No DQS to clock matching requirement.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

A/BA/cmd signals should be matched within 5 ps of CLK pairs.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MCP_MEM_COMP      | *     | Y                     | 7 MIL              | 7 MIL              | =STANDARD           | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| MCP_MEM_COMP     | *     | 8 MIL                | ?      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.3.4

Memory Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE     |              |                   |       |
|---------------------------|--------------|--------------|-------------------|-------|
|                           | PHYSICAL     | SPACING      |                   |       |
| MEM_A_CLK                 | MEM_70D_VDD  | MEM_CLK      | MEM A CLK P<5..0> | 15 28 |
| MEM_A_CLK                 | MEM_70D_VDD  | MEM_CLK      | MEM A CLK N<5..0> | 15 28 |
| MEM_A_CNTRL               | MEM_40S_VDD  | MEM_CTRL     | MEM A CKE<3..0>   | 15 28 |
| MEM_A_CNTRL               | MEM_40S_VDD  | MEM_CTRL     | MEM A CS_L<3..0>  | 15 28 |
| MEM_A_CNTRL               | MEM_40S_VDD  | MEM_CTRL     | MEM A ODT<3..0>   | 15 28 |
| MEM_A_CMD                 | MEM_40S_VDD  | MEM_CMD      | MEM A A<14..0>    | 15 28 |
| MEM_A_CMD                 | MEM_40S_VDD  | MEM_CMD      | MEM A BA<2..0>    | 15 28 |
| MEM_A_CMD                 | MEM_40S_VDD  | MEM_CMD      | MEM A RAS_L       | 15 28 |
| MEM_A_CMD                 | MEM_40S_VDD  | MEM_CMD      | MEM A CAS_L       | 15 28 |
| MEM_A_CMD                 | MEM_40S_VDD  | MEM_CMD      | MEM A WE_L        | 15 28 |
| MEM_A_DQ_BYTE0            | MEM_40S      | MEM_DATA     | MEM A DQ<7..0>    | 15 28 |
| MEM_A_DQ_BYTE1            | MEM_40S      | MEM_DATA     | MEM A DQ<15..8>   | 15 28 |
| MEM_A_DQ_BYTE2            | MEM_40S      | MEM_DATA     | MEM A DQ<23..16>  | 15 28 |
| MEM_A_DQ_BYTE3            | MEM_40S      | MEM_DATA     | MEM A DQ<31..24>  | 15 28 |
| MEM_A_DQ_BYTE4            | MEM_40S      | MEM_DATA     | MEM A DQ<39..32>  | 15 28 |
| MEM_A_DQ_BYTE5            | MEM_40S      | MEM_DATA     | MEM A DQ<47..40>  | 15 28 |
| MEM_A_DQ_BYTE6            | MEM_40S      | MEM_DATA     | MEM A DQ<55..48>  | 15 28 |
| MEM_A_DQ_BYTE7            | MEM_40S      | MEM_DATA     | MEM A DQ<63..56>  | 15 28 |
| MEM_A_DQ_BYTE0            | MEM_40S      | MEM_DATA     | MEM A DM<0>       | 15 28 |
| MEM_A_DQ_BYTE1            | MEM_40S      | MEM_DATA     | MEM A DM<1>       | 15 28 |
| MEM_A_DQ_BYTE2            | MEM_40S      | MEM_DATA     | MEM A DM<2>       | 15 28 |
| MEM_A_DQ_BYTE3            | MEM_40S      | MEM_DATA     | MEM A DM<3>       | 15 28 |
| MEM_A_DQ_BYTE4            | MEM_40S      | MEM_DATA     | MEM A DM<4>       | 15 28 |
| MEM_A_DQ_BYTE5            | MEM_40S      | MEM_DATA     | MEM A DM<5>       | 15 28 |
| MEM_A_DQ_BYTE6            | MEM_40S      | MEM_DATA     | MEM A DM<6>       | 15 28 |
| MEM_A_DQ_BYTE7            | MEM_40S      | MEM_DATA     | MEM A DM<7>       | 15 28 |
| MEM_A_DQS0                | MEM_70D      | MEM_DQS      | MEM A DQS P<0>    | 15 28 |
| MEM_A_DQS0                | MEM_70D      | MEM_DQS      | MEM A DQS N<0>    | 15 28 |
| MEM_A_DQS1                | MEM_70D      | MEM_DQS      | MEM A DQS P<1>    | 15 28 |
| MEM_A_DQS1                | MEM_70D      | MEM_DQS      | MEM A DQS N<1>    | 15 28 |
| MEM_A_DQS2                | MEM_70D      | MEM_DQS      | MEM A DQS P<2>    | 15 28 |
| MEM_A_DQS2                | MEM_70D      | MEM_DQS      | MEM A DQS N<2>    | 15 28 |
| MEM_A_DQS3                | MEM_70D      | MEM_DQS      | MEM A DQS P<3>    | 15 28 |
| MEM_A_DQS3                | MEM_70D      | MEM_DQS      | MEM A DQS N<3>    | 15 28 |
| MEM_A_DQS4                | MEM_70D      | MEM_DQS      | MEM A DQS P<4>    | 15 28 |
| MEM_A_DQS4                | MEM_70D      | MEM_DQS      | MEM A DQS N<4>    | 15 28 |
| MEM_A_DQS5                | MEM_70D      | MEM_DQS      | MEM A DQS P<5>    | 15 28 |
| MEM_A_DQS5                | MEM_70D      | MEM_DQS      | MEM A DQS N<5>    | 15 28 |
| MEM_A_DQS6                | MEM_70D      | MEM_DQS      | MEM A DQS P<6>    | 15 28 |
| MEM_A_DQS6                | MEM_70D      | MEM_DQS      | MEM A DQS N<6>    | 15 28 |
| MEM_A_DQS7                | MEM_70D      | MEM_DQS      | MEM A DQS P<7>    | 15 28 |
| MEM_A_DQS7                | MEM_70D      | MEM_DQS      | MEM A DQS N<7>    | 15 28 |
| MEM_B_CLK                 | MEM_70D_VDD  | MEM_CLK      | MEM B CLK P<5..0> | 15 29 |
| MEM_B_CLK                 | MEM_70D_VDD  | MEM_CLK      | MEM B CLK N<5..0> | 15 29 |
| MEM_B_CNTRL               | MEM_40S_VDD  | MEM_CTRL     | MEM B CKE<3..0>   | 15 29 |
| MEM_B_CNTRL               | MEM_40S_VDD  | MEM_CTRL     | MEM B CS_L<3..0>  | 15 29 |
| MEM_B_CNTRL               | MEM_40S_VDD  | MEM_CTRL     | MEM B ODT<3..0>   | 15 29 |
| MEM_B_CMD                 | MEM_40S_VDD  | MEM_CMD      | MEM B A<14..0>    | 15 29 |
| MEM_B_CMD                 | MEM_40S_VDD  | MEM_CMD      | MEM B BA<2..0>    | 15 29 |
| MEM_B_CMD                 | MEM_40S_VDD  | MEM_CMD      | MEM B RAS_L       | 15 29 |
| MEM_B_CMD                 | MEM_40S_VDD  | MEM_CMD      | MEM B CAS_L       | 15 29 |
| MEM_B_CMD                 | MEM_40S_VDD  | MEM_CMD      | MEM B WE_L        | 15 29 |
| MEM_B_DQ_BYTE0            | MEM_40S      | MEM_DATA     | MEM B DQ<7..0>    | 15 29 |
| MEM_B_DQ_BYTE1            | MEM_40S      | MEM_DATA     | MEM B DQ<15..8>   | 15 29 |
| MEM_B_DQ_BYTE2            | MEM_40S      | MEM_DATA     | MEM B DQ<23..16>  | 15 29 |
| MEM_B_DQ_BYTE3            | MEM_40S      | MEM_DATA     | MEM B DQ<31..24>  | 15 29 |
| MEM_B_DQ_BYTE4            | MEM_40S      | MEM_DATA     | MEM B DQ<39..32>  | 15 29 |
| MEM_B_DQ_BYTE5            | MEM_40S      | MEM_DATA     | MEM B DQ<47..40>  | 15 29 |
| MEM_B_DQ_BYTE6            | MEM_40S      | MEM_DATA     | MEM B DQ<55..48>  | 15 29 |
| MEM_B_DQ_BYTE7            | MEM_40S      | MEM_DATA     | MEM B DQ<63..56>  | 15 29 |
| MEM_B_DQ_BYTE0            | MEM_40S      | MEM_DATA     | MEM B DM<0>       | 15 29 |
| MEM_B_DQ_BYTE1            | MEM_40S      | MEM_DATA     | MEM B DM<1>       | 15 29 |
| MEM_B_DQ_BYTE2            | MEM_40S      | MEM_DATA     | MEM B DM<2>       | 15 29 |
| MEM_B_DQ_BYTE3            | MEM_40S      | MEM_DATA     | MEM B DM<3>       | 15 29 |
| MEM_B_DQ_BYTE4            | MEM_40S      | MEM_DATA     | MEM B DM<4>       | 15 29 |
| MEM_B_DQ_BYTE5            | MEM_40S      | MEM_DATA     | MEM B DM<5>       | 15 29 |
| MEM_B_DQ_BYTE6            | MEM_40S      | MEM_DATA     | MEM B DM<6>       | 15 29 |
| MEM_B_DQ_BYTE7            | MEM_40S      | MEM_DATA     | MEM B DM<7>       | 15 29 |
| MEM_B_DQS0                | MEM_70D      | MEM_DQS      | MEM B DQS P<0>    | 15 29 |
| MEM_B_DQS0                | MEM_70D      | MEM_DQS      | MEM B DQS N<0>    | 15 29 |
| MEM_B_DQS1                | MEM_70D      | MEM_DQS      | MEM B DQS P<1>    | 15 29 |
| MEM_B_DQS1                | MEM_70D      | MEM_DQS      | MEM B DQS N<1>    | 15 29 |
| MEM_B_DQS2                | MEM_70D      | MEM_DQS      | MEM B DQS P<2>    | 15 29 |
| MEM_B_DQS2                | MEM_70D      | MEM_DQS      | MEM B DQS N<2>    | 15 29 |
| MEM_B_DQS3                | MEM_70D      | MEM_DQS      | MEM B DQS P<3>    | 15 29 |
| MEM_B_DQS3                | MEM_70D      | MEM_DQS      | MEM B DQS N<3>    | 15 29 |
| MEM_B_DQS4                | MEM_70D      | MEM_DQS      | MEM B DQS P<4>    | 15 29 |
| MEM_B_DQS4                | MEM_70D      | MEM_DQS      | MEM B DQS N<4>    | 15 29 |
| MEM_B_DQS5                | MEM_70D      | MEM_DQS      | MEM B DQS P<5>    | 15 29 |
| MEM_B_DQS5                | MEM_70D      | MEM_DQS      | MEM B DQS N<5>    | 15 29 |
| MEM_B_DQS6                | MEM_70D      | MEM_DQS      | MEM B DQS P<6>    | 15 29 |
| MEM_B_DQS6                | MEM_70D      | MEM_DQS      | MEM B DQS N<6>    | 15 29 |
| MEM_B_DQS7                | MEM_70D      | MEM_DQS      | MEM B DQS P<7>    | 15 29 |
| MEM_B_DQS7                | MEM_70D      | MEM_DQS      | MEM B DQS N<7>    | 15 29 |
| MCP_MEM_COMP              | MCP_MEM_COMP | MCP_MEM_COMP | MCP MEM COMP VDD  | 16    |
| MCP_MEM_COMP              | MCP_MEM_COMP | MCP_MEM_COMP | MCP MEM COMP GND  | 16    |

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Memory Constraints

SYNC\_MASTER=MUXGFX

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PCI-Express

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCIE_90D          | *     | =90_OHM_DIFF          | =90_OHM_DIFF       | =90_OHM_DIFF       | 13.1 MM             | =90_OHM_DIFF         | =90_OHM_DIFF      |
| CLK_PCIE_100D     | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| PCIE             | *     | =3X_DIELECTRIC       | ?      |
| CLK_PCIE         | *     | 20 MIL               | ?      |
| MCP_PEX_COMP     | *     | 8 MIL                | ?      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.4

Analog Video Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CRT_50S           | *     | =50_OHM_SE            | =50_OHM_SE         | =50_OHM_SE         | =50_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CRT              | *     | =4:1_SPACING         | ?      |
| CRT_2CRT         | *     | =STANDARD            | ?      |
| CRT_2CLK         | *     | 50 MIL               | ?      |
| CRT_2SWITCHER    | *     | 250 MIL              | ?      |
| CRT_SYNC         | *     | 16 MIL               | ?      |
| MCP_DAC_COMP     | *     | =2:1_SPACING         | ?      |

CRT signal single-ended impedance varies by location:

- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Sections 2.5.1 & 2.5.2.

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Digital Video Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| DP_100D           | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |
| LVDS_100D         | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |
| MCP_DV_COMP       | *     | ?                     | 20 MIL             | 20 MIL             | =STANDARD           | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| DISPLAYPORT      | *     | =3X_DIELECTRIC       | ?      |
| LVDS             | *     | =3X_DIELECTRIC       | ?      |

| SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|------------|----------------------|--------|
| DISPLAYPORT      | TOP,BOTTOM | =4X_DIELECTRIC       | ?      |
| LVDS             | TOP,BOTTOM | =4X_DIELECTRIC       | ?      |

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.  
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.  
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.  
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.  
SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SATA_100D         | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SATA             | *     | =4X_DIELECTRIC       | ?      |
| SATA_TERM        | *     | 8 MIL                | ?      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.7.1.

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| ELECTRICAL_CONSTRAINT_SET | NET_TYPE      |              |                          |         |
|---------------------------|---------------|--------------|--------------------------|---------|
|                           | PHYSICAL      | SPACING      |                          |         |
|                           | PCIE_90D      | PCIE         | PEG R2D P<15..0>         | 71      |
|                           | PCIE_90D      | PCIE         | PEG R2D N<15..0>         | 71      |
| PEG_R2D                   | PCIE_90D      | PCIE         | PEG R2D C P<15..0>       | 9 71    |
|                           | PCIE_90D      | PCIE         | PEG R2D C N<15..0>       | 9 71    |
| PEG_D2R                   | PCIE_90D      | PCIE         | PEG D2R P<15..0>         | 9 71    |
|                           | PCIE_90D      | PCIE         | PEG D2R N<15..0>         | 9 71    |
|                           | PCIE_90D      | PCIE         | PEG D2R C P<15..0>       | 71      |
|                           | PCIE_90D      | PCIE         | PEG D2R C N<15..0>       | 71      |
|                           | PCIE_90D      | PCIE         | PCIE MINI R2D P          | 7 31 96 |
|                           | PCIE_90D      | PCIE         | PCIE MINI R2D N          | 7 31 96 |
| PCIE_MINI_R2D             | PCIE_90D      | PCIE         | PCIE MINI R2D C P        | 17 31   |
|                           | PCIE_90D      | PCIE         | PCIE MINI R2D C N        | 17 31   |
| PCIE_MINI_D2R             | PCIE_90D      | PCIE         | PCIE MINI D2R P          | 7 17 31 |
|                           | PCIE_90D      | PCIE         | PCIE MINI D2R N          | 7 17 31 |
|                           | PCIE_90D      | PCIE         | PCIE FW R2D P            | 36      |
|                           | PCIE_90D      | PCIE         | PCIE FW R2D N            | 36      |
| PCIE_FW_R2D               | PCIE_90D      | PCIE         | PCIE FW R2D C P          | 17 36   |
|                           | PCIE_90D      | PCIE         | PCIE FW R2D C N          | 17 36   |
| PCIE_FW_D2R               | PCIE_90D      | PCIE         | PCIE FW D2R P            | 17 36   |
|                           | PCIE_90D      | PCIE         | PCIE FW D2R N            | 17 36   |
|                           | PCIE_90D      | PCIE         | PCIE FW D2R C P          | 36      |
|                           | PCIE_90D      | PCIE         | PCIE FW D2R C N          | 36      |
|                           | PCIE_90D      | PCIE         | PCIE EXCARD R2D P        | 96      |
|                           | PCIE_90D      | PCIE         | PCIE EXCARD R2D N        | 96      |
| PCIE_EXCARD_R2D           | PCIE_90D      | PCIE         | TP PCIE EXCARD R2D C P   | 9 17    |
|                           | PCIE_90D      | PCIE         | TP PCIE EXCARD R2D C N   | 9 17    |
| PCIE_EXCARD_D2R           | PCIE_90D      | PCIE         | TP PCIE EXCARD D2R P     | 9 17    |
|                           | PCIE_90D      | PCIE         | TP PCIE EXCARD D2R N     | 9 17    |
| MCP_PE0_REECLK            | CLK_PCIE_100D | CLK_PCIE     | PEG CLK100M P            | 17 71   |
|                           | CLK_PCIE_100D | CLK_PCIE     | PEG CLK100M N            | 17 71   |
| MCP_PE1_REECLK            | CLK_PCIE_100D | CLK_PCIE     | PCIE CLK100M MINI P      | 17 31   |
|                           | CLK_PCIE_100D | CLK_PCIE     | PCIE CLK100M MINI N      | 17 31   |
| MCP_PE2_REECLK            | CLK_PCIE_100D | CLK_PCIE     | PCIE CLK100M FW P        | 17 36   |
|                           | CLK_PCIE_100D | CLK_PCIE     | PCIE CLK100M FW N        | 17 36   |
| MCP_PE3_REECLK            | CLK_PCIE_100D | CLK_PCIE     | TP PCIE CLK100M EXCARD P | 9 17    |
|                           | CLK_PCIE_100D | CLK_PCIE     | TP PCIE CLK100M EXCARD N | 9 17    |
| MCP_PEX_CLK_COMP          |               | MCP_PEX_COMP | MCP PEX CLK COMP         | 17      |
| CRT_RED                   | CRT_50S       | CRT          | NC CRT IG R C PR         | 18 25   |
| CRT_GREEN                 | CRT_50S       | CRT          | NC CRT IG G Y Y          | 18 25   |
| CRT_BLUE                  | CRT_50S       | CRT          | NC CRT IG B COMP PB      | 18 25   |
| CRT_SYNC                  | CRT_50S       | CRT_SYNC     | NC CRT IG HSYNC          | 18 25   |
| CRT_SYNC                  | CRT_50S       | CRT_SYNC     | NC CRT IG VSYNC          | 18 25   |
| MCP_DAC_RSET              |               | MCP_DAC_COMP | NC MCP TV DAC RSET       | 18 25   |
| MCP_DAC_VREF              |               | MCP_DAC_COMP | NC MCP TV DAC VREF       | 18 25   |
| TMDS_IG_TXC               | DP_100D       | DISPLAYPORT  | TMDS IG TXC P            |         |
| TMDS_IG_TXC               | DP_100D       | DISPLAYPORT  | TMDS IG TXC N            |         |
| TMDS_IG_TXD               | DP_100D       | DISPLAYPORT  | TMDS IG TXD P<2..0>      |         |
| TMDS_IG_TXD               | DP_100D       | DISPLAYPORT  | TMDS IG TXD N<2..0>      |         |
| DP_ML                     | DP_100D       | DISPLAYPORT  | DP IG ML P<3..0>         | 9 81    |
| DP_ML                     | DP_100D       | DISPLAYPORT  | DP IG ML N<3..0>         | 9 81    |
| DP_AUX_CH                 | DP_100D       | DISPLAYPORT  | DP IG AUX CH P           | 18 81   |
| DP_AUX_CH                 | DP_100D       | DISPLAYPORT  | DP IG AUX CH N           | 18 81   |
| MCP_HDMI_RSET             | MCP_DV_COMP   |              | MCP HDMI RSET            | 18 25   |
| MCP_HDMI_VPROBE           | MCP_DV_COMP   |              | MCP HDMI VPROBE          | 18 25   |
| LVDS_IG_A_CLK             | LVDS_100D     | LVDS         | LVDS IG A CLK P          | 18 84   |
| LVDS_IG_A_CLK             | LVDS_100D     | LVDS         | LVDS IG A CLK N          | 18 84   |
| LVDS_IG_A_DATA            | LVDS_100D     | LVDS         | LVDS IG A DATA P<2..0>   | 18 84   |
| LVDS_IG_A_DATA            | LVDS_100D     | LVDS         | LVDS IG A DATA N<2..0>   | 18 84   |
| LVDS_IG_A_DATA3           | LVDS_100D     | LVDS         | NC LVDS IG A DATAP<3>    | 9 18    |
| LVDS_IG_A_DATA3           | LVDS_100D     | LVDS         | NC LVDS IG A DATAN<3>    | 9 18    |
| LVDS_IG_B_CLK             | LVDS_100D     | LVDS         | NC LVDS IG B CLKP        | 9 18    |
| LVDS_IG_B_CLK             | LVDS_100D     | LVDS         | NC LVDS IG B CLKN        | 9 18    |
| LVDS_IG_B_DATA            | LVDS_100D     | LVDS         | LVDS IG B DATA P<2..0>   | 18 84   |
| LVDS_IG_B_DATA            | LVDS_100D     | LVDS         | LVDS IG B DATA N<2..0>   | 18 84   |
| LVDS_IG_B_DATA3           | LVDS_100D     | LVDS         | NC LVDS IG B DATAP<3>    | 9 18    |
| LVDS_IG_B_DATA3           | LVDS_100D     | LVDS         | NC LVDS IG B DATAN<3>    | 9 18    |
| MCP_IFPAB_RSET            | MCP_DV_COMP   |              | MCP IFPAB RSET           | 18 25   |
| MCP_IFPAB_VPROBE          |               |              | MCP IFPAB VPROBE         | 18 25   |
| SATA_HDD_R2D              | SATA_100D     | SATA         | SATA HDD R2D C P         | 20 39   |
|                           | SATA_100D     | SATA         | SATA HDD R2D C N         | 20 39   |
|                           | SATA_100D     | SATA         | SATA HDD R2D P           | 7 39    |
|                           | SATA_100D     | SATA         | SATA HDD R2D N           | 7 39    |
| SATA_HDD_D2R              | SATA_100D     | SATA         | SATA HDD D2R P           | 20 39   |
|                           | SATA_100D     | SATA         | SATA HDD D2R N           | 20 39   |
|                           | SATA_100D     | SATA         | SATA HDD D2R C P         | 7 39    |
|                           | SATA_100D     | SATA         | SATA HDD D2R C N         | 7 39    |
| SATA_ODD_R2D              | SATA_100D     | SATA         | SATA ODD R2D C P         | 20 39   |
|                           | SATA_100D     | SATA         | SATA ODD R2D C N         | 20 39   |
|                           | SATA_100D     | SATA         | SATA ODD R2D P           | 7 39    |
|                           | SATA_100D     | SATA         | SATA ODD R2D N           | 7 39    |
| SATA_ODD_D2R              | SATA_100D     | SATA         | SATA ODD D2R P           | 20 39   |
|                           | SATA_100D     | SATA         | SATA ODD D2R N           | 20 39   |
|                           | SATA_100D     | SATA         | SATA ODD D2R C P         | 7 39    |
|                           | SATA_100D     | SATA         | SATA ODD D2R C N         | 7 39    |
| MCP_SATA_TERM             |               | SATA_TERM    | MCP SATA_TERM            | 20      |

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MCP Constraints 1

SYNC\_MASTER=MUXGFX SYNC\_DATE=02/18/2008

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PCI Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCI_55S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |
| CLK_PCI_55S       | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| PCI              | *     | =STANDARD            | ?      |
| CLK_PCI          | *     | 8 MIL                | ?      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.8.

LPC Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| LPC_55S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |
| CLK_LPC_55S       | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| LPC              | *     | 6 MIL                | ?      |
| CLK_LPC          | *     | 8 MIL                | ?      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MCP_USB_RBBIAS    | *     | =STANDARD             | 8 MIL              | 8 MIL              | =STANDARD           | =STANDARD            | =STANDARD         |
| USB_90D           | *     | =90_OHM_DIFF          | =90_OHM_DIFF       | =90_OHM_DIFF       | =90_OHM_DIFF        | =90_OHM_DIFF         | =90_OHM_DIFF      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| USB              | *     | =2x_DIELECTRIC       | ?      | USB              | TOP,BOTTOM | =4x_DIELECTRIC       | ?      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.10.1.

SMBus Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SMB_55S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SMB              | *     | =2x_DIELECTRIC       | ?      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.11.1.

HD Audio Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| HDA_55S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| HDA              | *     | =2x_DIELECTRIC       | ?      |
| MCP_HDA_COMP     | *     | 8 MIL                | ?      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.12.1.

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SIO Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CLK_SLOW_55S      | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CLK_SLOW         | *     | 8 MIL                | ?      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.13.

SPI Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SPI_55S           | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SPI              | *     | 8 MIL                | ?      |

SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Section 2.14.

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| ELECTRICAL_CONSTRAINT_SET | NET_TYPE       |          |                                 |
|---------------------------|----------------|----------|---------------------------------|
|                           | PHYSICAL       | SPACING  |                                 |
| MCP_DEBUG                 | PCI_55S        | PCI      | MCP_DEBUG<7..0> 13 19           |
| PCI_AD                    | PCI_55S        | PCI      | PCI_AD<23..8>                   |
| PCI_AD24                  | PCI_55S        | PCI      | PCI_AD<24>                      |
| PCI_AD                    | PCI_55S        | PCI      | PCI_AD<31..25>                  |
| PCI_AD                    | PCI_55S        | PCI      | PCI_PAR                         |
| PCI_C_BE_L                | PCI_55S        | PCI      | PCI_C_BE_L<3..0>                |
| PCI_CNTRL                 | PCI_55S        | PCI      | PCI_IRDY_L                      |
| PCI_CNTRL                 | PCI_55S        | PCI      | PCI_DEVSEL_L                    |
| PCI_CNTRL                 | PCI_55S        | PCI      | PCI_PERR_L                      |
| PCI_CNTRL                 | PCI_55S        | PCI      | PCI_SERR_L                      |
| PCI_CNTRL                 | PCI_55S        | PCI      | PCI_STOP_L                      |
| PCI_CNTRL                 | PCI_55S        | PCI      | PCI_TRDY_L                      |
| PCI_CNTRL                 | PCI_55S        | PCI      | PCI_FRAME_L                     |
| PCI_REQ0_L                | PCI_55S        | PCI      | PCI_REQ0_L 19                   |
| PCI_GNT0_L                | PCI_55S        | PCI      | PCI_GNT0_L                      |
| PCI_REQ1_L                | PCI_55S        | PCI      | PCI_REQ1_L 19                   |
| PCI_GNT1_L                | PCI_55S        | PCI      | PCI_GNT1_L                      |
| PCI_INTW_L                | PCI_55S        | PCI      | PCI_INTW_L                      |
| PCI_INTX_L                | PCI_55S        | PCI      | PCI_INTX_L                      |
| PCI_INTY_L                | PCI_55S        | PCI      | PCI_INTY_L                      |
| PCI_INTZ_L                | PCI_55S        | PCI      | PCI_INTZ_L                      |
| MCP_PCI_CLK2              | CLK_PCI_55S    | CLK_PCI  | PCI_CLK33M MCP_R 19             |
|                           | CLK_PCI_55S    | CLK_PCI  | PCI_CLK33M MCP 19               |
| LPC_AD                    | LPC_55S        | LPC      | LPC_AD<3..0> 19 42 44 84        |
| LPC_FRAME_L               | LPC_55S        | LPC      | LPC_FRAME_L 19 42 44 84         |
| LPC_RESET_L               | LPC_55S        | LPC      | LPC_RESET_L 19 26 84            |
| MCP_LPC_CLK0              | CLK_LPC_55S    | CLK_LPC  | LPC_CLK33M SMC_R 19 26          |
|                           | CLK_LPC_55S    | CLK_LPC  | LPC_CLK33M SMC 26 42            |
|                           | CLK_LPC_55S    | CLK_LPC  | LPC_CLK33M LPCPLUS 26 44        |
| USB_EXTN_P                | USB_90D        | USB      | USB_EXTN_P 20 40                |
| USB_EXTN_N                | USB_90D        | USB      | USB_EXTN_N 20 40                |
| USB_EXTN_MUXED_P          | USB_90D        | USB      | USB_EXTN_MUXED_P                |
| USB_EXTN_MUXED_N          | USB_90D        | USB      | USB_EXTN_MUXED_N                |
| NC_USB_MINIP              | USB_90D        | USB      | NC_USB_MINIP 9 20               |
| NC_USB_MININ              | USB_90D        | USB      | NC_USB_MININ 9 20               |
| NC_USB_EXTDP              | USB_90D        | USB      | NC_USB_EXTDP 9 20               |
| NC_USB_EXTDN              | USB_90D        | USB      | NC_USB_EXTDN 9 20               |
| USB_CAMERA_P              | USB_90D        | USB      | USB_CAMERA_P 7 20 31            |
| USB_CAMERA_N              | USB_90D        | USB      | USB_CAMERA_N 7 20 31            |
| USB_BT_P                  | USB_90D        | USB      | USB_BT_P 7 20 31                |
| USB_BT_N                  | USB_90D        | USB      | USB_BT_N 7 20 31                |
| USB_TPAD_P                | USB_90D        | USB      | USB_TPAD_P 20 50                |
| USB_TPAD_N                | USB_90D        | USB      | USB_TPAD_N 20 50                |
| USB_IR_P                  | USB_90D        | USB      | USB_IR_P 20 41                  |
| USB_IR_N                  | USB_90D        | USB      | USB_IR_N 20 41                  |
| USB_EXTB_P                | USB_90D        | USB      | USB_EXTB_P 20 40                |
| USB_EXTB_N                | USB_90D        | USB      | USB_EXTB_N 20 40                |
| NC_USB_EXCARDP            | USB_90D        | USB      | NC_USB_EXCARDP 9 20             |
| NC_USB_EXCARDN            | USB_90D        | USB      | NC_USB_EXCARDN 9 20             |
| NC_USB_EXTCP              | USB_90D        | USB      | NC_USB_EXTCP 9 20               |
| NC_USB_EXTCN              | USB_90D        | USB      | NC_USB_EXTCN 9 20               |
| MCP_USB_RBBIAS            | MCP_USB_RBBIAS |          | MCP_USB_RBBIAS_GND 20           |
| SMBUS_MCP_0_CLK           | SMB_55S        | SMB      | SMBUS_MCP_0_CLK 13 21 28 29 45  |
| SMBUS_MCP_0_DATA          | SMB_55S        | SMB      | SMBUS_MCP_0_DATA 13 21 28 29 45 |
| SMBUS_MCP_1_CLK           | SMB_55S        | SMB      | SMBUS_MCP_1_CLK 21 45 60 85     |
| SMBUS_MCP_1_DATA          | SMB_55S        | SMB      | SMBUS_MCP_1_DATA 21 45 60 85    |
| HDA_BIT_CLK               | HDA_55S        | HDA      | HDA_BIT_CLK 21 55               |
| HDA_BIT_CLK_R             | HDA_55S        | HDA      | HDA_BIT_CLK_R 21                |
| HDA_SYNC                  | HDA_55S        | HDA      | HDA_SYNC 21 55                  |
| HDA_RST_L                 | HDA_55S        | HDA      | HDA_RST_R_L 21                  |
| HDA_RST_L                 | HDA_55S        | HDA      | HDA_RST_L 21 55                 |
| HDA_SDIN0                 | HDA_55S        | HDA      | HDA_SDIN0 21 55                 |
| HDA_SDIN0                 | HDA_55S        | HDA      | HDA_SDIN_CODEC 21 55            |
| HDA_SDOUT                 | HDA_55S        | HDA      | HDA_SDOUT 21 55                 |
| HDA_SDOUT                 | HDA_55S        | HDA      | HDA_SDOUT_R 21                  |
| MCP_HDA_PULLDN_COMP       | MCP_HDA_COMP   |          | MCP_HDA_PULLDN_COMP 21          |
| PM_CLK32K_SUSCLK_R        | CLK_SLOW_55S   | CLK_SLOW | PM_CLK32K_SUSCLK_R 21 26        |
| PM_CLK32K_SUSCLK          | CLK_SLOW_55S   | CLK_SLOW | PM_CLK32K_SUSCLK 26 42          |
| SPI_CLK                   | SPI_55S        | SPI      | SPI_CLK_R 21 44                 |
| SPI_CLK                   | SPI_55S        | SPI      | SPI_CLK 54                      |
| SPI_MOSI                  | SPI_55S        | SPI      | SPI_MOSI_R 21 44                |
| SPI_MOSI                  | SPI_55S        | SPI      | SPI_MOSI 54                     |
| SPI_MISO                  | SPI_55S        | SPI      | SPI_MISO 21 44                  |
| SPI_MISO                  | SPI_55S        | SPI      | SPI_MISO_R 54                   |
| SPI_CS0                   | SPI_55S        | SPI      | SPI_CS0_R_L 21 44               |
| SPI_CS0                   | SPI_55S        | SPI      | SPI_CS0_L                       |

MCP Constraints 2

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MCP RGMII (Ethernet) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MCP_MII_COMP      | *     | =STANDARD             | 7.5 MIL            | 7.5 MIL            | =STANDARD           | =STANDARD            | =STANDARD         |
| ENET_MII_55S      | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| MCP_BUF0_CLK     | *     | =3:1_SPACING         | ?      |
| ENET_MII         | *     | 12 MIL               | ?      |






















SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| ENET_MDI_100D     | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| ENET_MDI         | *     | 25 MIL               | ?      |

SOURCE: MCP73 Interface DG (DG-02974-001\_v01), Section 2.7.4

| ELECTRICAL_CONSTRAINT_SET                                                                                | NET_TYPE      |              |                        |       |
|----------------------------------------------------------------------------------------------------------|---------------|--------------|------------------------|-------|
|                                                                                                          | PHYSICAL      | SPACING      |                        |       |
|  MCP_MII_COMP         | MCP_MII_COMP  |              | MCP MII COMP VDD       | 16    |
|  MCP_MII_COMP         | MCP_MII_COMP  |              | MCP MII COMP GND       | 16    |
|  MCP_CLK25M_BUF0      | ENET_MII_55S  | MCP_BUF0_CLK | MCP_CLK25M_BUF0_R      | 16 34 |
|  MCP_CLK25M_BUF0      | ENET_MII_55S  | MCP_BUF0_CLK | RTL8211 CLK25M CKXTAL1 | 33 34 |
|  ENET_INTR_L          | ENET_MII_55S  | ENET_MII     | ENET_INTR_L            |       |
|  ENET_MDIO            | ENET_MII_55S  | ENET_MII     | ENET MDIO              | 16 33 |
|  ENET_MDC             | ENET_MII_55S  | ENET_MII     | ENET MDC               | 16 33 |
|  ENET_PWRDWN_L        | ENET_MII_55S  | ENET_MII     | ENET_PWRDWN_L          |       |
|  ENET_CLK125M_RXCLK_R | ENET_MII_55S  | ENET_MII     | ENET_CLK125M_RXCLK_R   | 33    |
|  ENET_RXCLK           | ENET_MII_55S  | ENET_MII     | ENET_CLK125M_RXCLK     | 16 33 |
|  ENET_RXD             | ENET_MII_55S  | ENET_MII     | ENET_RXD R<3..0>       | 33    |
|  ENET_RXD             | ENET_MII_55S  | ENET_MII     | ENET_RXD<0>            | 16 33 |
|  ENET_RXD_STRAP       | ENET_MII_55S  | ENET_MII     | ENET_RXD<3..1>         | 16 33 |
|  ENET_RXD             | ENET_MII_55S  | ENET_MII     | ENET_RX_CTRL           | 16 33 |
|  ENET_TXCLK           | ENET_MII_55S  | ENET_MII     | ENET_CLK125M_TXCLK     | 16 33 |
|  ENET_TXD0            | ENET_MII_55S  | ENET_MII     | ENET_TXD<0>            | 16 33 |
|  ENET_TXD             | ENET_MII_55S  | ENET_MII     | ENET_TXD<3..1>         | 16 33 |
|  ENET_TXD             | ENET_MII_55S  | ENET_MII     | ENET_TX_CTRL           | 16 33 |
|  ENET_RESET_L         | ENET_MII_55S  | ENET_MII     | ENET_RESET_L           | 16 33 |
|  ENET_MDI             | ENET_MDI_100D | ENET_MDI     | ENET MDI P<3..0>       | 33 36 |
|  ENET_MDI             | ENET_MDI_100D | ENET_MDI     | ENET MDI N<3..0>       | 33 36 |

Ethernet Constraints

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FireWire Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| FW_110D           | *     | =110_OHM_DIFF         | =110_OHM_DIFF      | =110_OHM_DIFF      | =110_OHM_DIFF       | =110_OHM_DIFF        | =110_OHM_DIFF     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| FW_TP            | *     | =3:1_SPACING         | ?      |

SD CARD INTERFACE CONSTRAINTS

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SD_55S            | *     | =55_OHM_SE            | =55_OHM_SE         | =55_OHM_SE         | =55_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SD_INTERFACE     | *     | =3X_DIELECTRIC       | ?      |

FireWire Net Properties

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE |         |                |       |
|---------------------------|----------|---------|----------------|-------|
|                           | PHYSICAL | SPACING |                |       |
| FW_P0_TPA                 | FW_110D  | FW_TP   | NC FW0 TPAP    | 36 38 |
| FW_P0_TPAN                | FW_110D  | FW_TP   | NC FW0 TPAN    | 36 38 |
| FW_P0_TPBP                | FW_110D  | FW_TP   | NC FW0 TPBP    | 36 38 |
| FW_P0_TPBN                | FW_110D  | FW_TP   | NC FW0 TPBN    | 36 38 |
| FW_P1_TPA_P               | FW_110D  | FW_TP   | FW PORT1 TPA P | 36 38 |
| FW_P1_TPA_N               | FW_110D  | FW_TP   | FW PORT1 TPA N | 36 38 |
| FW_P1_TPB_P               | FW_110D  | FW_TP   | FW PORT1 TPB P | 36 38 |
| FW_P1_TPB_N               | FW_110D  | FW_TP   | FW PORT1 TPB N | 36 38 |
| Port 2 Not Used           |          |         |                |       |

SD CARD NET PROPERTIES

| ELECTRICAL_CONSTRAINT_SET | NET_TYPE |              |         |      |
|---------------------------|----------|--------------|---------|------|
|                           | PHYSICAL | SPACING      |         |      |
| SD_DATA                   | SD_55S   | SD_INTERFACE | SD_D<0> | 7 32 |
| SD_DATA                   | SD_55S   | SD_INTERFACE | SD_D<1> | 7 32 |
| SD_DATA                   | SD_55S   | SD_INTERFACE | SD_D<2> | 7 32 |
| SD_DATA                   | SD_55S   | SD_INTERFACE | SD_D<3> | 7 32 |
| SD_DATA                   | SD_55S   | SD_INTERFACE | SD_D<4> | 7 32 |
| SD_DATA                   | SD_55S   | SD_INTERFACE | SD_D<5> | 7 32 |
| SD_DATA                   | SD_55S   | SD_INTERFACE | SD_D<6> | 7 32 |
| SD_DATA                   | SD_55S   | SD_INTERFACE | SD_D<7> | 7 32 |
| SD_CLK                    | SD_55S   | SD_INTERFACE | SD_CLK  | 7 32 |
| SD_CMD                    | SD_55S   | SD_INTERFACE | SD_CMD  | 7 32 |

FireWire Constraints

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






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| PHYSICAL_RULE_SET | LAYER | ALLOW_ROUTE_ON_LAYER? | MINIMUM_LINE_WIDTH | MINIMUM_NECK_WIDTH | MAXIMUM_NECK_LENGTH | DIFFPAIR_PRIMARY_GAP | DIFFPAIR_NECK_GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| 1TO1_DIFFPAIR     | *     | =STANDARD             | =STANDARD          | =STANDARD          | =STANDARD           | 0.1 MM               | 0.1 MM            |

SMC SMBus Net Properties

| NET_TYPE                                                                                               |          |         |                    |                |
|--------------------------------------------------------------------------------------------------------|----------|---------|--------------------|----------------|
| ELECTRICAL_CONSTRAINT_SET                                                                              | PHYSICAL | SPACING |                    |                |
|  SMBUS_SMC_A_S3_SCL | SMB_55S  | SMB     | SMBUS_SMC_A_S3_SCL | 7 31 42 45 51  |
|  SMBUS_SMC_A_S3_SDA | SMB_55S  | SMB     | SMBUS_SMC_A_S3_SDA | 7 31 42 45 51  |
|  SMBUS_SMC_B_S0_SCL | SMB_55S  | SMB     | SMBUS_SMC_B_S0_SCL | 42 45 48       |
|  SMBUS_SMC_B_S0_SDA | SMB_55S  | SMB     | SMBUS_SMC_B_S0_SDA | 42 45 48       |
|  SMBUS_SMC_0_S0_SCL | SMB_55S  | SMB     | SMBUS_SMC_0_S0_SCL | 42 45 48 53 78 |
|  SMBUS_SMC_0_S0_SDA | SMB_55S  | SMB     | SMBUS_SMC_0_S0_SDA | 42 45 48 53 78 |
|  SMBUS_SMC_BSA_SCL  | SMB_55S  | SMB     | SMBUS_SMC_BSA_SCL  | 7 42 45 61 62  |
|  SMBUS_SMC_BSA_SDA  | SMB_55S  | SMB     | SMBUS_SMC_BSA_SDA  | 7 42 45 61 62  |
|  SMBUS_SMC_MGMT_SCL | SMB_55S  | SMB     | SMBUS_SMC_MGMT_SCL | 27 39 42 45    |
|  SMBUS_SMC_MGMT_SDA | SMB_55S  | SMB     | SMBUS_SMC_MGMT_SDA | 27 39 42 45    |

SMBus Charger Net Properties

| NET_TYPE                                                                                     |               |         |            |    |
|----------------------------------------------------------------------------------------------|---------------|---------|------------|----|
| ELECTRICAL_CONSTRAINT_SET                                                                    | PHYSICAL      | SPACING |            |    |
|  CHGR_CSI | 1TO1_DIFFPAIR |         | CHGR_CSI_P | 62 |
|  CHGR_CSI | 1TO1_DIFFPAIR |         | CHGR_CSI_N | 62 |
|  CHGR_CSO | 1TO1_DIFFPAIR |         | CHGR_CSO_P | 62 |
|  CHGR_CSO | 1TO1_DIFFPAIR |         | CHGR_CSO_N | 62 |

SMC Constraints

SYNC\_MASTER=MUXGFX SYNC\_DATE=02/18/2008

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APPLE INC.

SIZE  
D

DRAWING NUMBER  
051-7892

REV.

A.0.0

SCALE  
NONE

SHT  
94

OF  
97



GDDR3 Frame Buffer Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| GDDR3_40R55SE     | *     | =45_OHM_SE            | =40_OHM_SE         | 0.095 MM           | 12.7 MM             | =STANDARD            | =STANDARD         |
| GDDR3_40SE        | *     | =45_OHM_SE            | =40_OHM_SE         | 0.095 MM           | =40_OHM_SE          | =STANDARD            | =STANDARD         |
| GDDR3_80D         | *     | =40_OHM_DIFF          | =40_OHM_DIFF       | 0.095 MM           | =40_OHM_DIFF        | =40_OHM_DIFF         | =40_OHM_DIFF      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| GDDR3_CLK        | *     | =2.5:1_SPACING       | ?      |
| GDDR3_CMD        | *     | =2.5:1_SPACING       | ?      |
| GDDR3_DATA       | *     | =2.5:1_SPACING       | ?      |
| GDDR3_DQS        | *     | =2.5:1_SPACING       | ?      |

From T18 MXM:

Digital Video Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| DP_100D           | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |
| LVDS_100D         | *     | =100_OHM_DIFF         | =100_OHM_DIFF      | =100_OHM_DIFF      | =100_OHM_DIFF       | =100_OHM_DIFF        | =100_OHM_DIFF     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| DISPLAYPORT      | *     | =3x_DIELECTRIC       | ?      | DISPLAYPORT      | TOP,BOTTOM | =4x_DIELECTRIC       | ?      |
| LVDS             | *     | =3x_DIELECTRIC       | ?      | LVDS             | TOP,BOTTOM | =4x_DIELECTRIC       | ?      |

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.  
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.  
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.  
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.  
SOURCE: MCP79 Interface DG (DG-03328-001\_v0D), Sections 2.5.3 & 2.5.4.

MUXGFX Net Properties

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL  | SPACING     | NET_TYPE                 |
|---------------------------|-----------|-------------|--------------------------|
| LVDS_A_CLK                | LVDS_100D | LVDS        | LVDS_A_CLK_P             |
| LVDS_A_CLK                | LVDS_100D | LVDS        | LVDS_A_CLK_N             |
| LVDS_A_DATA               | LVDS_100D | LVDS        | LVDS_A_DATA_P<2..0>      |
| LVDS_A_DATA               | LVDS_100D | LVDS        | LVDS_A_DATA_N<2..0>      |
| LVDS_B_CLK                | LVDS_100D | LVDS        | LVDS_B_CLK_P             |
| LVDS_B_CLK                | LVDS_100D | LVDS        | LVDS_B_CLK_N             |
| LVDS_B_DATA               | LVDS_100D | LVDS        | LVDS_B_DATA_P<2..0>      |
| LVDS_B_DATA               | LVDS_100D | LVDS        | LVDS_B_DATA_N<2..0>      |
| LVDS_CONN_A_CLK_F_P       | LVDS_100D | LVDS        | LVDS_CONN_A_CLK_F_P      |
| LVDS_CONN_A_CLK_F_N       | LVDS_100D | LVDS        | LVDS_CONN_A_CLK_F_N      |
| LVDS_CONN_B_CLK_F_P       | LVDS_100D | LVDS        | LVDS_CONN_B_CLK_F_P      |
| LVDS_CONN_B_CLK_F_N       | LVDS_100D | LVDS        | LVDS_CONN_B_CLK_F_N      |
| LVDS_CONN_A_CLK_P         | LVDS_100D | LVDS        | LVDS_CONN_A_CLK_P        |
| LVDS_CONN_A_CLK_N         | LVDS_100D | LVDS        | LVDS_CONN_A_CLK_N        |
| LVDS_CONN_A_DATA_P<2..0>  | LVDS_100D | LVDS        | LVDS_CONN_A_DATA_P<2..0> |
| LVDS_CONN_A_DATA_N<2..0>  | LVDS_100D | LVDS        | LVDS_CONN_A_DATA_N<2..0> |
| LVDS_CONN_B_CLK_P         | LVDS_100D | LVDS        | LVDS_CONN_B_CLK_P        |
| LVDS_CONN_B_CLK_N         | LVDS_100D | LVDS        | LVDS_CONN_B_CLK_N        |
| LVDS_CONN_B_DATA_P<2..0>  | LVDS_100D | LVDS        | LVDS_CONN_B_DATA_P<2..0> |
| LVDS_CONN_B_DATA_N<2..0>  | LVDS_100D | LVDS        | LVDS_CONN_B_DATA_N<2..0> |
| DP_ML                     | DP_100D   | DISPLAYPORT | DP_ML_C_P<3..0>          |
| DP_ML                     | DP_100D   | DISPLAYPORT | DP_ML_C_N<3..0>          |
| DP_ML                     | DP_100D   | DISPLAYPORT | DP_ML_CONN_P<3..0>       |
| DP_ML                     | DP_100D   | DISPLAYPORT | DP_ML_CONN_N<3..0>       |
| DP_ML                     | DP_100D   | DISPLAYPORT | DP_ML_CONN_P<3..0>       |
| DP_ML                     | DP_100D   | DISPLAYPORT | DP_ML_CONN_N<3..0>       |
| DP_AUX_CH                 | DP_100D   | DISPLAYPORT | DP_AUX_CH_C_P            |
| DP_AUX_CH                 | DP_100D   | DISPLAYPORT | DP_AUX_CH_C_N            |

GDDR3 FB A/B Net Properties

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL      | SPACING    | NET_TYPE        |
|---------------------------|---------------|------------|-----------------|
| FB_A_CLK_P                | GDDR3_80D     | GDDR3_CLK  | FB A_CLK_P<0>   |
| FB_A_CLK_P                | GDDR3_80D     | GDDR3_CLK  | FB A_CLK_N<0>   |
| FB_B_CLK_P                | GDDR3_80D     | GDDR3_CLK  | FB A_CLK_P<1>   |
| FB_B_CLK_P                | GDDR3_80D     | GDDR3_CLK  | FB A_CLK_N<1>   |
| FB_AB_CMD                 | GDDR3_40R55SE | GDDR3_CMD  | FB A_MA<1..0>   |
| FB_AB_CMD                 | GDDR3_40R55SE | GDDR3_CMD  | FB A_MA<12..6>  |
| FB_AB_CMD                 | GDDR3_40R55SE | GDDR3_CMD  | FB A_BA<2..0>   |
| FB_AB_CMD                 | GDDR3_40R55SE | GDDR3_CMD  | FB A_RAS_L      |
| FB_AB_CMD                 | GDDR3_40R55SE | GDDR3_CMD  | FB A_CAS_L      |
| FB_AB_CMD                 | GDDR3_40R55SE | GDDR3_CMD  | FB A_WE_L       |
| FB_AB_CMD_PD              | GDDR3_40R55SE | GDDR3_CMD  | FB A_UCKE       |
| FB_AB_CMD_PD              | GDDR3_40R55SE | GDDR3_CMD  | FB A_LCKE       |
| FB_AB_CMD_PD              | GDDR3_40R55SE | GDDR3_CMD  | FB A_LCS0_L     |
| FB_AB_CMD_PD              | GDDR3_40R55SE | GDDR3_CMD  | FB A_DRAM_RST   |
| FB_A_CMD                  | GDDR3_40SE    | GDDR3_CMD  | FB A_LMA<5..2>  |
| FB_B_CMD                  | GDDR3_40SE    | GDDR3_CMD  | FB A_UMA<5..2>  |
| FB_A_WDQS0                | GDDR3_40SE    | GDDR3_DQS  | FB A_WDQS<0>    |
| FB_A_WDQS1                | GDDR3_40SE    | GDDR3_DQS  | FB A_WDQS<1>    |
| FB_A_WDQS2                | GDDR3_40SE    | GDDR3_DQS  | FB A_WDQS<2>    |
| FB_A_WDQS3                | GDDR3_40SE    | GDDR3_DQS  | FB A_WDQS<3>    |
| FB_A_RDQS0                | GDDR3_40SE    | GDDR3_DQS  | FB A_RDQS<0>    |
| FB_A_RDQS1                | GDDR3_40SE    | GDDR3_DQS  | FB A_RDQS<1>    |
| FB_A_RDQS2                | GDDR3_40SE    | GDDR3_DQS  | FB A_RDQS<2>    |
| FB_A_RDQS3                | GDDR3_40SE    | GDDR3_DQS  | FB A_RDQS<3>    |
| FB_A_DQ_BYTE0             | GDDR3_40SE    | GDDR3_DATA | FB A_DQ<7..0>   |
| FB_A_DQ_BYTE1             | GDDR3_40SE    | GDDR3_DATA | FB A_DQ<15..8>  |
| FB_A_DQ_BYTE2             | GDDR3_40SE    | GDDR3_DATA | FB A_DQ<23..16> |
| FB_A_DQ_BYTE3             | GDDR3_40SE    | GDDR3_DATA | FB A_DQ<31..24> |
| FB_A_DQM0                 | GDDR3_40SE    | GDDR3_DATA | FB A_DQM_L<0>   |
| FB_A_DQM1                 | GDDR3_40SE    | GDDR3_DATA | FB A_DQM_L<1>   |
| FB_A_DQM2                 | GDDR3_40SE    | GDDR3_DATA | FB A_DQM_L<2>   |
| FB_A_DQM3                 | GDDR3_40SE    | GDDR3_DATA | FB A_DQM_L<3>   |
| FB_B_WDQS0                | GDDR3_40SE    | GDDR3_DQS  | FB A_WDQS<4>    |
| FB_B_WDQS1                | GDDR3_40SE    | GDDR3_DQS  | FB A_WDQS<5>    |
| FB_B_WDQS2                | GDDR3_40SE    | GDDR3_DQS  | FB A_WDQS<6>    |
| FB_B_WDQS3                | GDDR3_40SE    | GDDR3_DQS  | FB A_WDQS<7>    |
| FB_B_RDQS0                | GDDR3_40SE    | GDDR3_DQS  | FB A_RDQS<4>    |
| FB_B_RDQS1                | GDDR3_40SE    | GDDR3_DQS  | FB A_RDQS<5>    |
| FB_B_RDQS2                | GDDR3_40SE    | GDDR3_DQS  | FB A_RDQS<6>    |
| FB_B_RDQS3                | GDDR3_40SE    | GDDR3_DQS  | FB A_RDQS<7>    |
| FB_B_DQ_BYTE0             | GDDR3_40SE    | GDDR3_DATA | FB A_DQ<39..32> |
| FB_B_DQ_BYTE1             | GDDR3_40SE    | GDDR3_DATA | FB A_DQ<47..40> |
| FB_B_DQ_BYTE2             | GDDR3_40SE    | GDDR3_DATA | FB A_DQ<55..48> |
| FB_B_DQ_BYTE3             | GDDR3_40SE    | GDDR3_DATA | FB A_DQ<63..56> |
| FB_B_DQM0                 | GDDR3_40SE    | GDDR3_DATA | FB A_DQM_L<4>   |
| FB_B_DQM1                 | GDDR3_40SE    | GDDR3_DATA | FB A_DQM_L<5>   |
| FB_B_DQM2                 | GDDR3_40SE    | GDDR3_DATA | FB A_DQM_L<6>   |
| FB_B_DQM3                 | GDDR3_40SE    | GDDR3_DATA | FB A_DQM_L<7>   |

G96 Net Properties

| ELECTRICAL_CONSTRAINT_SET | PHYSICAL     | SPACING     | NET_TYPE               |
|---------------------------|--------------|-------------|------------------------|
| GPU_CLK27M                | CLK_SLOW_55S | CLK_SLOW    | GPU_CLK27M             |
| GPU_CLK27M_SS             | CLK_SLOW_55S | CLK_SLOW    | GPU_CLK27M_SS          |
| LVDS_EG_A_CLK_P           | LVDS_100D    | LVDS        | LVDS_EG_A_CLK_P        |
| LVDS_EG_A_CLK_N           | LVDS_100D    | LVDS        | LVDS_EG_A_CLK_N        |
| LVDS_EG_A_DATA_P<2..0>    | LVDS_100D    | LVDS        | LVDS_EG_A_DATA_P<2..0> |
| LVDS_EG_A_DATA_N<2..0>    | LVDS_100D    | LVDS        | LVDS_EG_A_DATA_N<2..0> |
| LVDS_EG_B_DATA_P<2..0>    | LVDS_100D    | LVDS        | LVDS_EG_B_DATA_P<2..0> |
| LVDS_EG_B_DATA_N<2..0>    | LVDS_100D    | LVDS        | LVDS_EG_B_DATA_N<2..0> |
| DP_ML                     | DP_100D      | DISPLAYPORT | DP_EG_ML_P<3..0>       |
| DP_ML                     | DP_100D      | DISPLAYPORT | DP_EG_ML_N<3..0>       |
| DP_AUX_CH                 | DP_100D      | DISPLAYPORT | DP_EG_AUX_CH_P         |
| DP_AUX_CH                 | DP_100D      | DISPLAYPORT | DP_EG_AUX_CH_N         |
| DP_AUX_CH                 | DP_100D      | DISPLAYPORT | DP_EG_AUX_CH_C_P       |
| DP_AUX_CH                 | DP_100D      | DISPLAYPORT | DP_EG_AUX_CH_C_N       |

GDDR3 FB C/D Net Properties

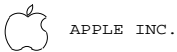
| ELECTRICAL_CONSTRAINT_SET | PHYSICAL      | SPACING    | NET_TYPE        |
|---------------------------|---------------|------------|-----------------|
| FB_C_CLK_P                | GDDR3_80D     | GDDR3_CLK  | FB B_CLK_P<0>   |
| FB_C_CLK_P                | GDDR3_80D     | GDDR3_CLK  | FB B_CLK_N<0>   |
| FB_D_CLK_P                | GDDR3_80D     | GDDR3_CLK  | FB B_CLK_P<1>   |
| FB_D_CLK_P                | GDDR3_80D     | GDDR3_CLK  | FB B_CLK_N<1>   |
| FB_CD_CMD                 | GDDR3_40R55SE | GDDR3_CMD  | FB B_MA<1..0>   |
| FB_CD_CMD                 | GDDR3_40R55SE | GDDR3_CMD  | FB B_MA<12..6>  |
| FB_CD_CMD                 | GDDR3_40R55SE | GDDR3_CMD  | FB B_BA<2..0>   |
| FB_CD_CMD                 | GDDR3_40R55SE | GDDR3_CMD  | FB B_RAS_L      |
| FB_CD_CMD                 | GDDR3_40R55SE | GDDR3_CMD  | FB B_CAS_L      |
| FB_CD_CMD                 | GDDR3_40R55SE | GDDR3_CMD  | FB B_WE_L       |
| FB_CD_CMD_PD              | GDDR3_40R55SE | GDDR3_CMD  | FB B_UCKE       |
| FB_CD_CMD_PD              | GDDR3_40R55SE | GDDR3_CMD  | FB B_LCKE       |
| FB_CD_CMD_PD              | GDDR3_40R55SE | GDDR3_CMD  | FB B_LCS0_L     |
| FB_CD_CMD_PD              | GDDR3_40R55SE | GDDR3_CMD  | FB B_DRAM_RST   |
| FB_C_CMD                  | GDDR3_40SE    | GDDR3_CMD  | FB B_LMA<5..2>  |
| FB_D_CMD                  | GDDR3_40SE    | GDDR3_CMD  | FB B_UMA<5..2>  |
| FB_C_WDQS0                | GDDR3_40SE    | GDDR3_DQS  | FB B_WDQS<0>    |
| FB_C_WDQS1                | GDDR3_40SE    | GDDR3_DQS  | FB B_WDQS<1>    |
| FB_C_WDQS2                | GDDR3_40SE    | GDDR3_DQS  | FB B_WDQS<2>    |
| FB_C_WDQS3                | GDDR3_40SE    | GDDR3_DQS  | FB B_WDQS<3>    |
| FB_C_RDQS0                | GDDR3_40SE    | GDDR3_DQS  | FB B_RDQS<0>    |
| FB_C_RDQS1                | GDDR3_40SE    | GDDR3_DQS  | FB B_RDQS<1>    |
| FB_C_RDQS2                | GDDR3_40SE    | GDDR3_DQS  | FB B_RDQS<2>    |
| FB_C_RDQS3                | GDDR3_40SE    | GDDR3_DQS  | FB B_RDQS<3>    |
| FB_C_DQ_BYTE0             | GDDR3_40SE    | GDDR3_DATA | FB B_DQ<7..0>   |
| FB_C_DQ_BYTE1             | GDDR3_40SE    | GDDR3_DATA | FB B_DQ<15..8>  |
| FB_C_DQ_BYTE2             | GDDR3_40SE    | GDDR3_DATA | FB B_DQ<23..16> |
| FB_C_DQ_BYTE3             | GDDR3_40SE    | GDDR3_DATA | FB B_DQ<31..24> |
| FB_C_DQM0                 | GDDR3_40SE    | GDDR3_DATA | FB B_DQM_L<0>   |
| FB_C_DQM1                 | GDDR3_40SE    | GDDR3_DATA | FB B_DQM_L<1>   |
| FB_C_DQM2                 | GDDR3_40SE    | GDDR3_DATA | FB B_DQM_L<2>   |
| FB_C_DQM3                 | GDDR3_40SE    | GDDR3_DATA | FB B_DQM_L<3>   |
| FB_D_WDQS0                | GDDR3_40SE    | GDDR3_DQS  | FB B_WDQS<4>    |
| FB_D_WDQS1                | GDDR3_40SE    | GDDR3_DQS  | FB B_WDQS<5>    |
| FB_D_WDQS2                | GDDR3_40SE    | GDDR3_DQS  | FB B_WDQS<6>    |
| FB_D_WDQS3                | GDDR3_40SE    | GDDR3_DQS  | FB B_WDQS<7>    |
| FB_D_RDQS0                | GDDR3_40SE    | GDDR3_DQS  | FB B_RDQS<4>    |
| FB_D_RDQS1                | GDDR3_40SE    | GDDR3_DQS  | FB B_RDQS<5>    |
| FB_D_RDQS2                | GDDR3_40SE    | GDDR3_DQS  | FB B_RDQS<6>    |
| FB_D_RDQS3                | GDDR3_40SE    | GDDR3_DQS  | FB B_RDQS<7>    |
| FB_D_DQ_BYTE0             | GDDR3_40SE    | GDDR3_DATA | FB B_DQ<39..32> |
| FB_D_DQ_BYTE1             | GDDR3_40SE    | GDDR3_DATA | FB B_DQ<47..40> |
| FB_D_DQ_BYTE2             | GDDR3_40SE    | GDDR3_DATA | FB B_DQ<55..48> |
| FB_D_DQ_BYTE3             | GDDR3_40SE    | GDDR3_DATA | FB B_DQ<63..56> |
| FB_D_DQM0                 | GDDR3_40SE    | GDDR3_DATA | FB B_DQM_L<4>   |
| FB_D_DQM1                 | GDDR3_40SE    | GDDR3_DATA | FB B_DQM_L<5>   |
| FB_D_DQM2                 | GDDR3_40SE    | GDDR3_DATA | FB B_DQM_L<6>   |
| FB_D_DQM3                 | GDDR3_40SE    | GDDR3_DATA | FB B_DQM_L<7>   |

GPU (G96) CONSTRAINTS

SYNC\_MASTER=MUXGFX SYNC\_DATE=02/18/2008

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|       |                |       |
|-------|----------------|-------|
| SIZE  | DRAWING NUMBER | REV.  |
| D     | 051-7892       | A.0.0 |
| SCALE | SHT            | OF    |
| NONE  | 95             | 97    |







|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|---------------------------------------------------------------------------|--|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|----------------------------|------------------|--------------------|-------|----------------------|--------|-------------------|--|-------------------|-----------|------------------|
| 8                                                                         |  | 7     |                       | 6                  |                    | 5                   |                      | 4                          |                  | 3                  |       | 2                    |        | 1                 |  |                   |           |                  |
| K19 Board-Specific Spacing & Physical Constraints                         |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
| BOARD LAYERS                                                              |  |       |                       |                    |                    | BOARD AREAS         |                      | BOARD UNITS<br>(MIL or MM) |                  | ALLEGRO<br>VERSION |       |                      |        |                   |  |                   |           |                  |
| TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM |  |       |                       |                    |                    | NO_TYPE, BGA, PGA   |                      | MM                         |                  | 15.5.1             |       |                      |        |                   |  |                   |           |                  |
| PHYSICAL_RULE_SET                                                         |  | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP          | SPACING_RULE_SET |                    | LAYER | LINE-TO-LINE SPACING | WEIGHT | NET_SPACING_TYPE1 |  | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
| DEFAULT                                                                   |  | *     | Y                     | ~50_OHM_SE         | ~50_OHM_SE         | 33.6 MM             | 0 MM                 | 0 MM                       | DEFAULT          |                    | *     | 0.1 MM               | ?      | *                 |  | *                 | BGA       | BGA_P1MM         |
| STANDARD                                                                  |  | *     | Y                     | ~DEFAULT           | ~DEFAULT           | 10 MM               | ~DEFAULT             | ~DEFAULT                   | STANDARD         |                    | *     | ~DEFAULT             | ?      | MEM_CLK           |  | *                 | BGA       | BGA_P2MM         |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            | BGA_P1MM         |                    | *     | ~DEFAULT             | ?      | CLK_FSB           |  | *                 | BGA       | BGA_P2MM         |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            | BGA_P2MM         |                    | *     | ~DEFAULT             | ?      | CLK_PCIE          |  | *                 | BGA       | BGA_P2MM         |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            | BGA_P3MM         |                    | *     | ~DEFAULT             | ?      | CLK_SLOW          |  | *                 | BGA       | BGA_P2MM         |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            | PGA_CPU          |                    | *     | 0.073 MM             | ?      | FSB_DSTB          |  | FSB_DSTB          | BGA       | BGA_P3MM         |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
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|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
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|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
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|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
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|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
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|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
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|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
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|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
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|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
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|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |
|                                                                           |  |       |                       |                    |                    |                     |                      |                            |                  |                    |       |                      |        |                   |  |                   |           |                  |

PCB Rule Definitions

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SYNC\_DATE=01/22/2008


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